IBM Digital Logic Card Data Sheets

IBM
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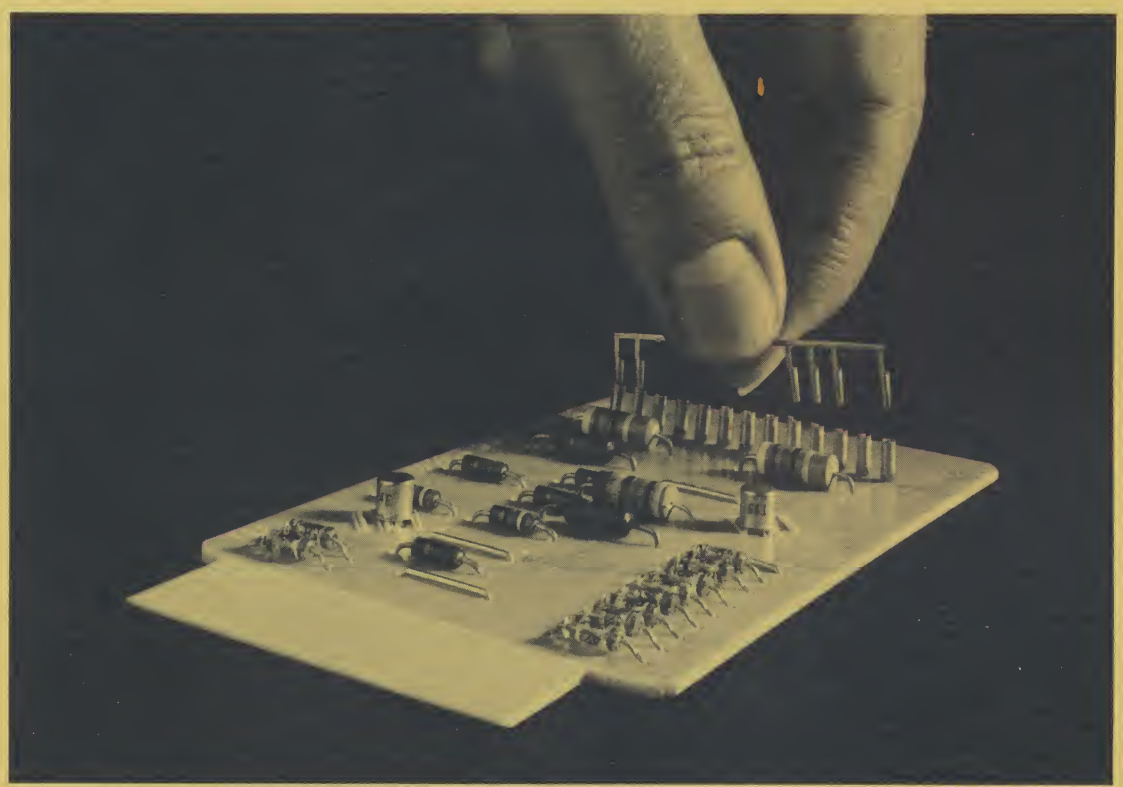
PRODUCT

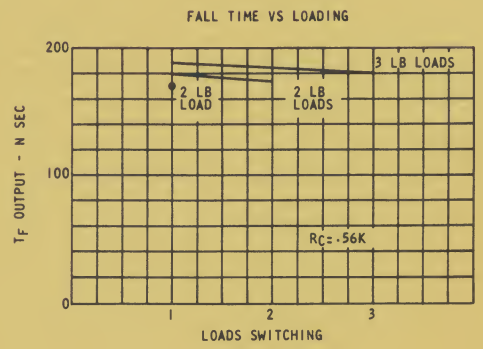
The IBM digital logic circuit card family comprises a complete line of printed cards for electronics logic functions. Five of the cards are programmable; that is, five cards of the family can easily be converted to perform the functions of many different circuit configurations. The remaining cards of the family are discrete cards.

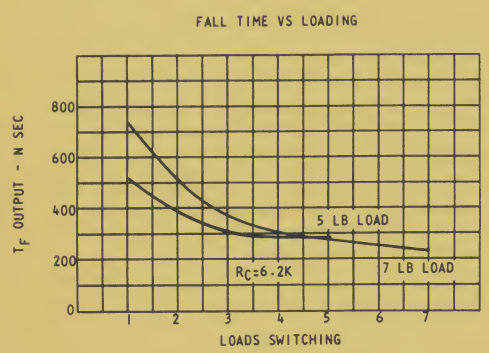
Features:

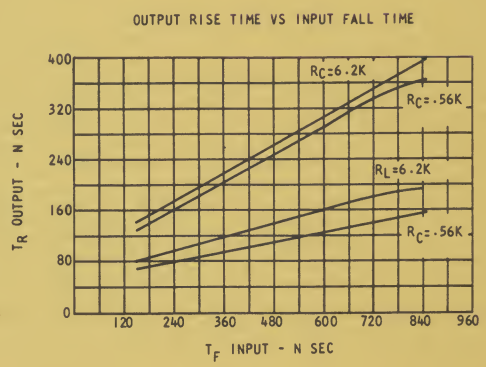
- ☐ High performance characteristics
- ☐ Internal circuit flexibility
- ☐ Logic card versatility
- ☐ Simplified circuit design
- ☐ Programmable for various loading conditions
- ☐ High-speed/low-speed switching
- ☐ Marginal checking
- ☐ Proven operating characteristics
- ☐ Simplified circuit modifications

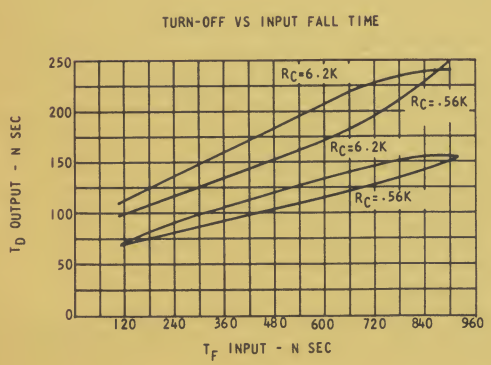


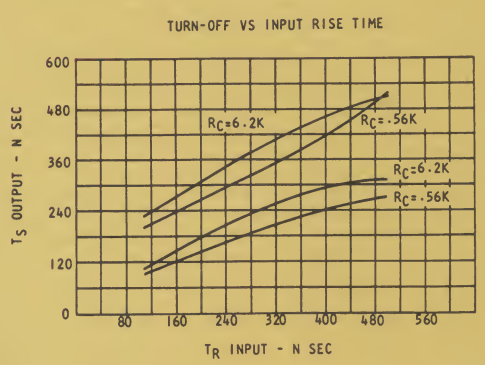
LOW SPEED SINGLE LEVEL LOGIC BLOCKS











Ordering Information

Terms: 30 days net, f.o.b. point of shipment. Requests for price quotation and other inquiries should be directed to IBM Industrial Products, 1000 Westchester Avenue, White Plains, New York 10604. This includes requirements and specifications other than those shown in this publication.

Please specify: 1. IBM part number. 2. Method of shipment. 3. Required delivery date. 4. Special instructions, including tax exemption qualifications. (Specifications and prices subject to change without notice.)

As part of the process of continuing product improvement, IBM reserves the right to make changes in specifications or performance, at any time, without notification to past customers.

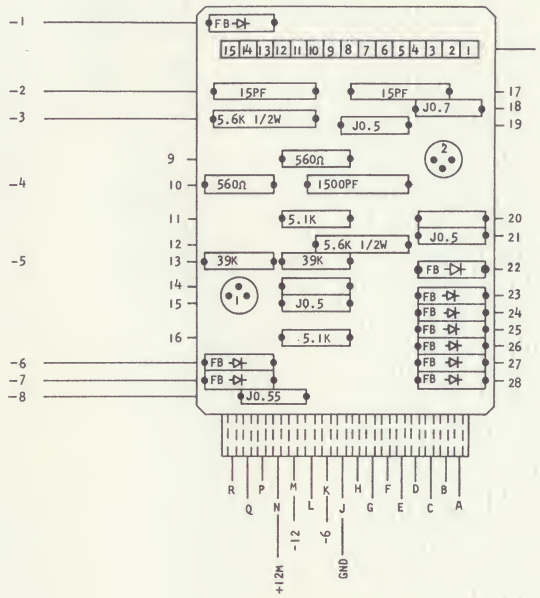
Form No. 560-0111-00. Litho in

P/N 370955
6Y**

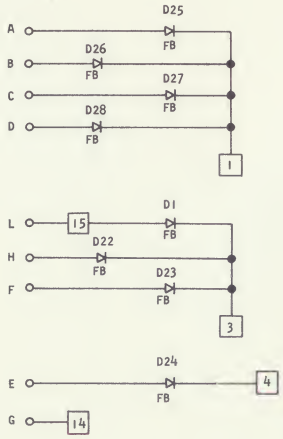
PROGRAMMABLE CARD, SINGLE LEVEL

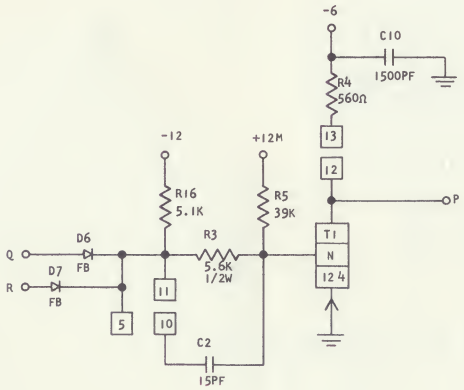
CIRCUIT NAME	CAP CODE	ASM. NO	TEST SPEC	CARD CODE
2-5 WAY (-A) LOADS	JU	372589	870585	ZGL-
2-5 WAY (-A) WITHOUT LOADS	JV	372590	870585	ZGM-
1-10 WAY (-A)	JW	372591	870585	ZGN-
10 WAY LOGIC BLOCK LOW SPEED W/LOAD	JX	370373	892380	DGZ-
10 WAY LOGIC BLOCK LOW SPEED WO/LOAD	JY	370374	892380	DHA-
5 WAY LOGIC BLOCK LOW SPEED WO/LOAD	JZ	370375	892380	DGY-
5 WAY LOGIC BLOCK LOW SPEED W/LOAD	JM	370376	892380	DGX-
1-6 WAY, 1-4 WAY WO/LOAD (-A)	LW	372123	892216	DHV-
1-8 WAY AND 1-2 WAY WO/LOAD	LX	372193	892216	DHY-
1-8 WAY AND 1-2 WAY W/LOAD	LY	372194	892380	DHZ-
1-6 WAY, 1-4 WAY W/LOAD (-A)	LZ	372195	892380	DEN-
1-6 WAY, 1-4 WAY (-A) WO/LOAD H.S.	MZ	372528	8922.6	DKY-

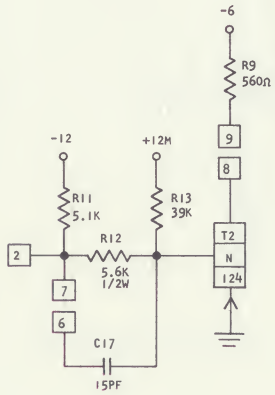
CAP CONFIGURATION

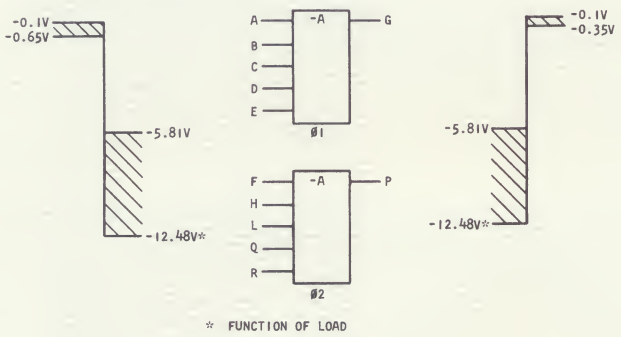


COMPONENT SIDE









* FUNCTION OF LOAD

OTHER DESIGNATIONS

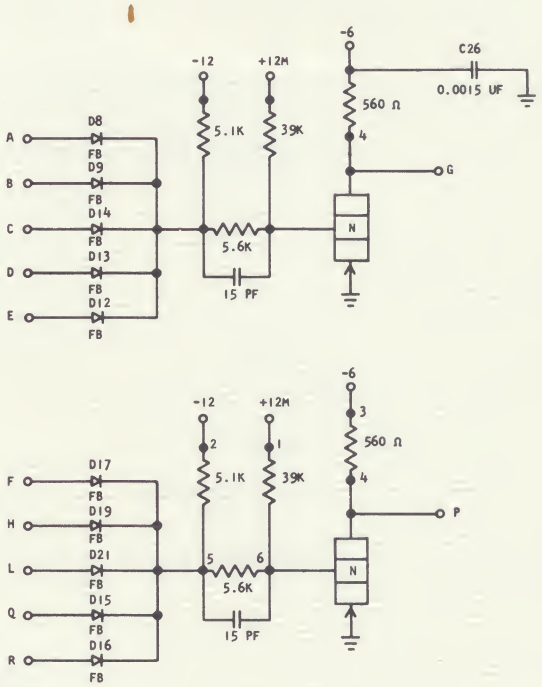
+0, -A0, +0A, +00, I, IO, IA

SEQUENCE OF OPERATION

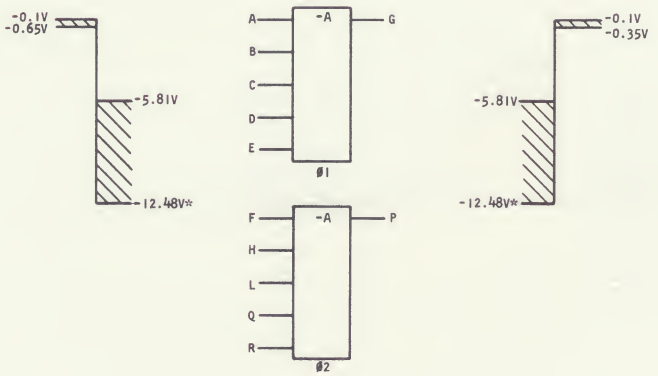
1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	18	100
TURN OFF (NSEC)	15	150



2-Five Input NAND Gates, without load h.s. (SLLB #1) Ref. Eng. Spec. 870585



* FUNCTION OF LOAD

OTHER DESIGNATIONS

+0, -A0, +0A, +00, I, I0, IA

SEQUENCE OF OPERATION

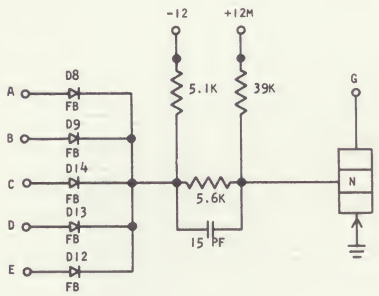
1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

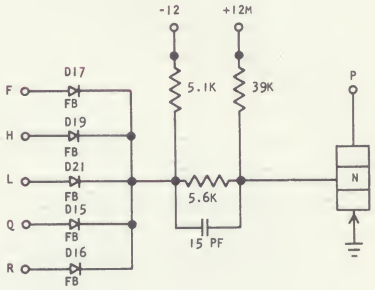
DELAY

WITH 560Ω OR 1.6K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	18	100*
TURN OFF (NSEC)	15	150**

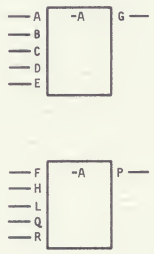
* THIS DELAY CAN INCREASE TO 180 NSEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.
** THIS DELAY CAN INCREASE TO 200 NSEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

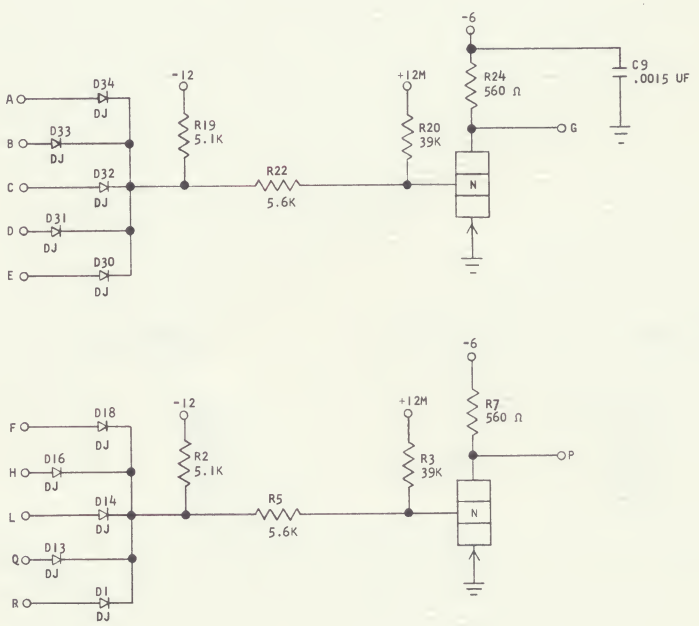




2-Five Input NAND Gates, with load 1.s. (SLLB #1)

Ref. Eng. Spec. DGX-892380





SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A,F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C,L	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
D,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
E,R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G,P	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY: SDTDL - LOW SPEED

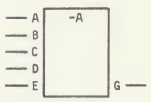
LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

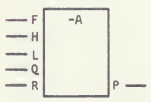
	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

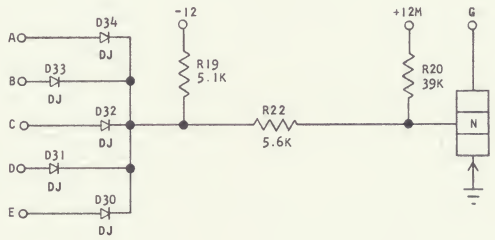
*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

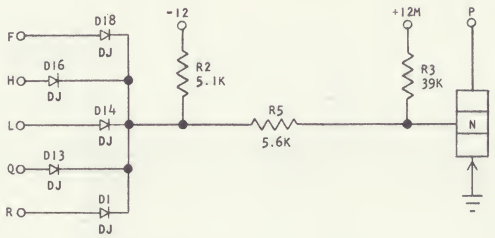
**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

2-Five Input NAND Gates, without load l.s. (SLLB #1) Ref. Eng. Spec. DGY-892380









SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A,F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
B,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
C,L	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
D,Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
E,R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.8	-8.8
G,P	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

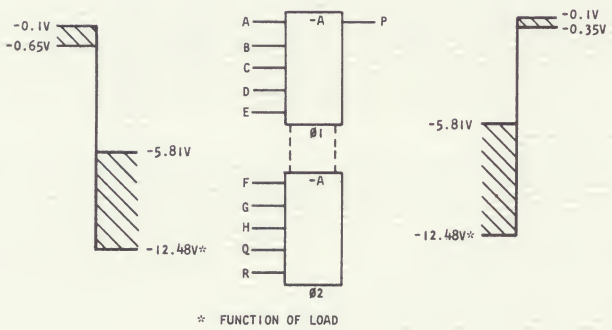
	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

1-Ten Input NAND Gate, with load, h.s. (SLLB #1)

Ref. Eng. Spec. 870585



* FUNCTION OF LOAD

OTHER DESIGNATIONS

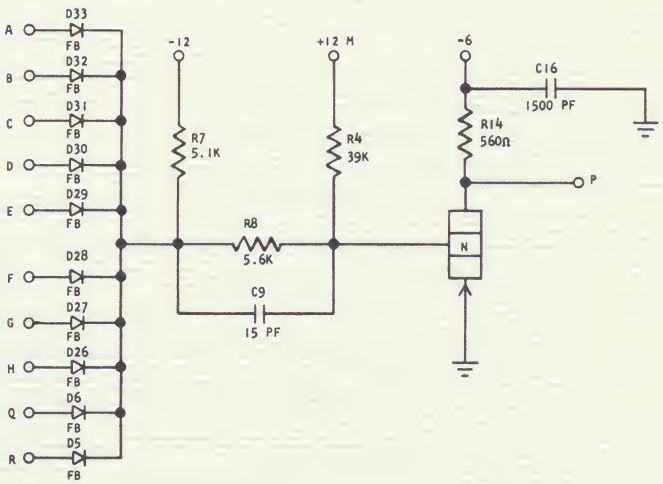
+0, -A0, +0A, +00, I, I0, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

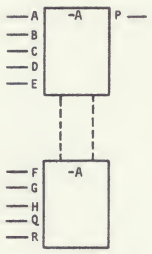
DELAY

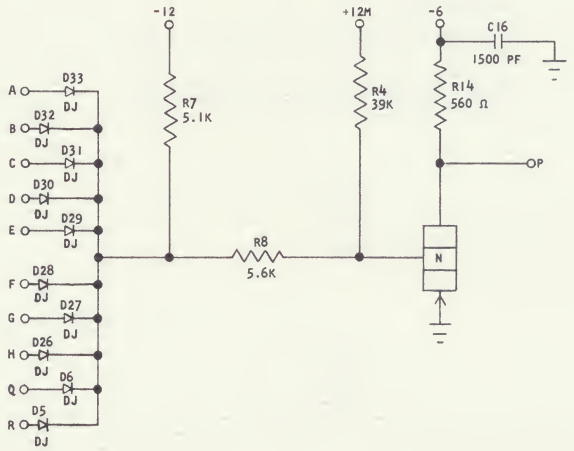
	MIN	MAX
TURN ON (NSEC)	18	100
TURN OFF (NSEC)	15	150



1-Ten Input NAND Gate, with load, l.s. (SLLB #1)

Ref. Eng. Spec. 892380





DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
E	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
P	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

1-Ten Input NAND Gate, without load, l.s. (SLLB #1)

Ref. Eng. Spec. 892380

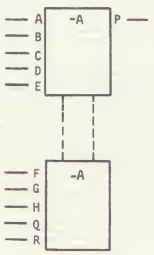
DELAY: SDTDL - LOW SPEED

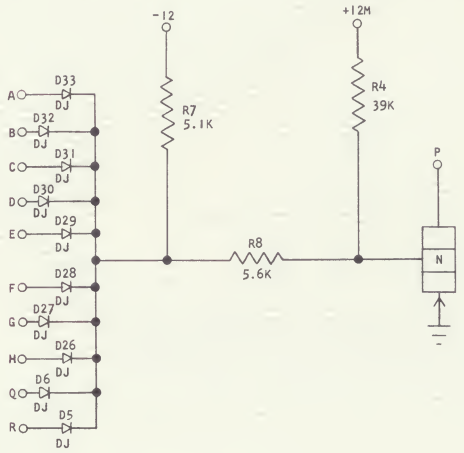
LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.





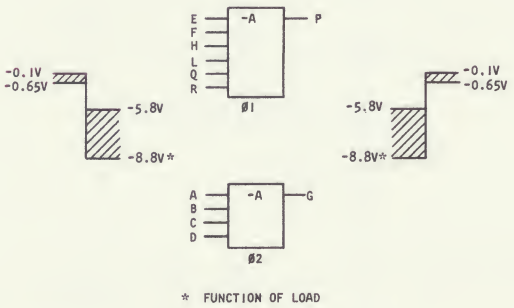
SEQUENCE OF OPERATION

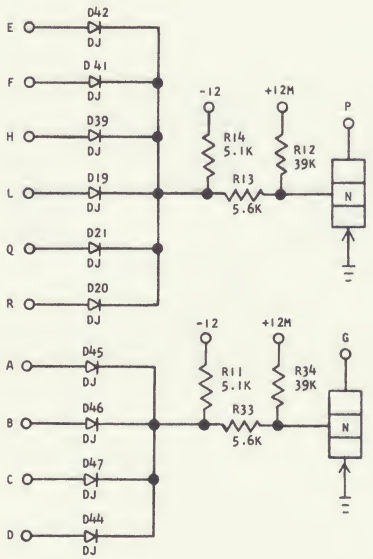
1. ALL INPUTS DOWN TRANSISTOR ON OUTPUT UP.
2. ANY INPUT UP TRANSISTOR OFF OUTPUT DOWN.
3. COLLECTOR MUST BE LOADED.
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN	MAX
A	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
B	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
C	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
D	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
E	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
F	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
G	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
Q	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
R	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
P	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

1-Six Input and 1-Four Input NAND Gate, without loads, l.s. (SLLB #1)

DHV-
Ref. Eng. Spec. 892380





OTHER DESIGNATIONS:

+0, -A0, +0A, +00, I, IO, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.

2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

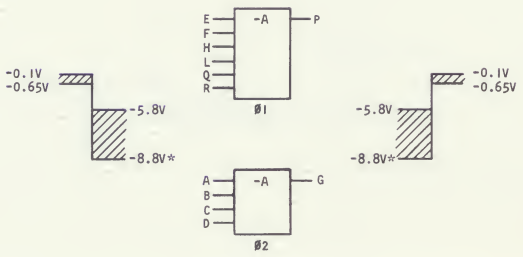
	MIN	MAX
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

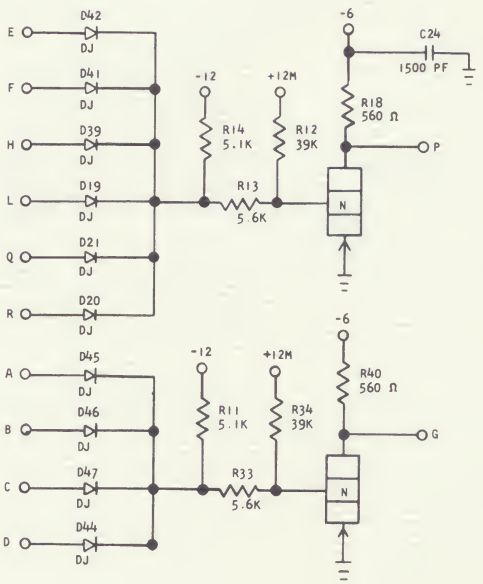
**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

1-Six Input and 1-Four Input NAND Gate, with loads, l.s. (SLLB #1)

DEN-
Ref. Eng. Spec. 892380



* FUNCTION OF LOAD



OTHER DESIGNATIONS:

+0, -A0, +0A, +00, I, ID, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.

2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY

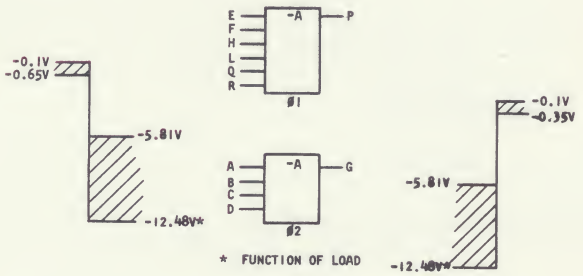
	MIN	MAX
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

1-Six Input and 1-Four Input NAND Gate, without loads, h.s. (SLLB #1)

DKY-
Ref. Eng. Spec. 870585



* FUNCTION OF LOAD

OTHER DESIGNATIONS

+0, -A0, +0A, +00, I, I0, IA

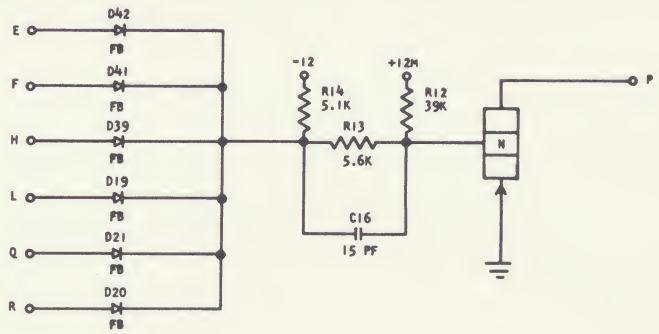
SEQUENCE OF OPERATION

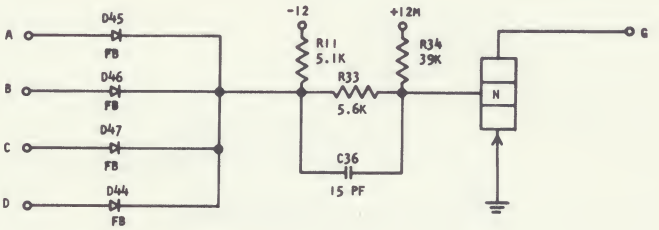
1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY	MIN	MAX
WITH 560 Ω OR 1.6K COLLECTOR RESISTOR		
TURN ON (NSEC)	18	100*
TURN OFF (NSEC)	15	150**

*THIS DELAY CAN INCREASE TO 180 N SEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

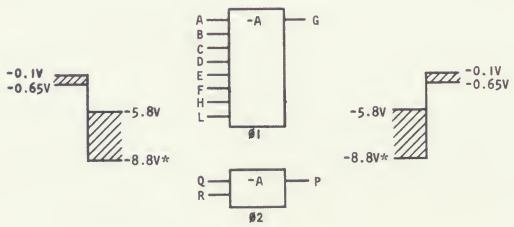
**THIS DELAY CAN INCREASE TO 200 N SEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.



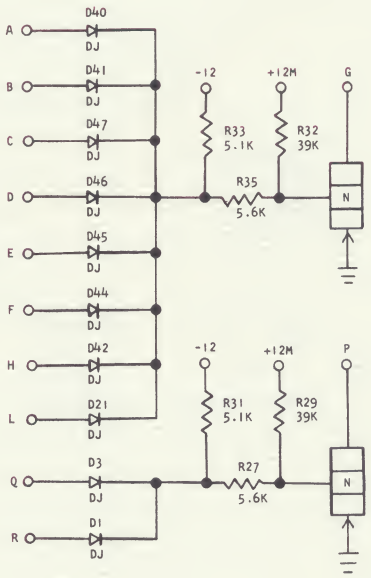


1-Eight Input and 1-Two Input NAND Gate, without load, l.s. (SLLB #1)

DHY-
Ref. Eng. Spec. 892380



* FUNCTION OF LOAD



OTHER DESIGNATIONS:

+0, -A0, +0A, +00, I, I0, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.

2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

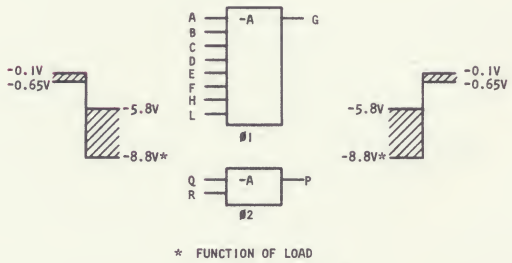
	MIN	MAX
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

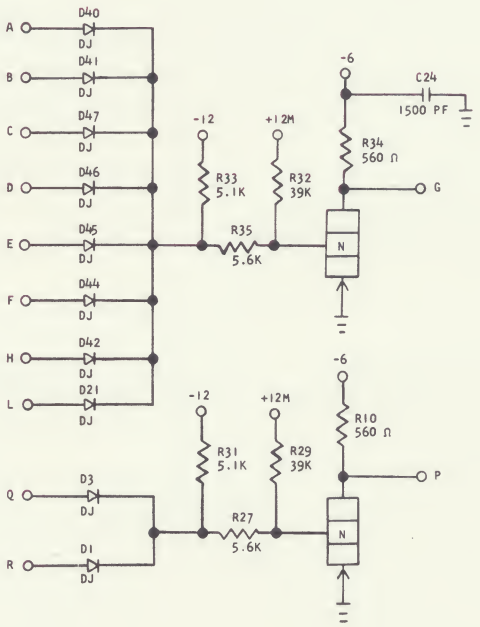
**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

1-Eight Input and 1-Two Input NAND Gate, with load, l.s. (SLLB #1)

DHZ-
Ref. Eng. Spec. 892380



* FUNCTION OF LOAD



OTHER DESIGNATIONS:

+0, -A0, +0A, +00, I, I0, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP

2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN

DELAY

	MIN	MAX
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

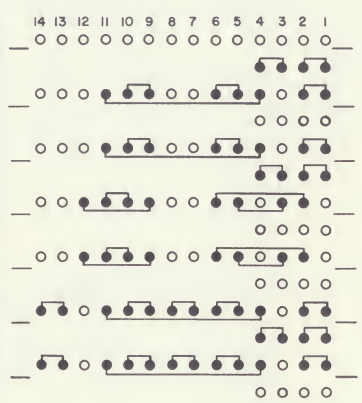
**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

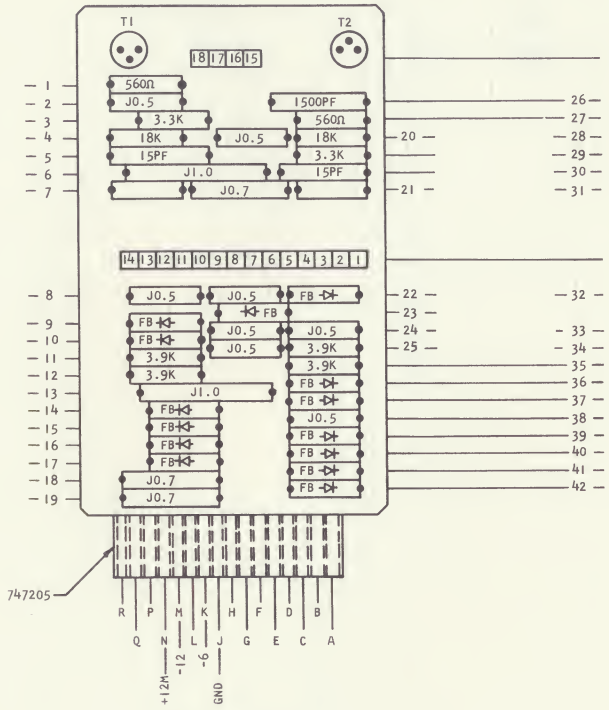
P/N 370952
3Y**

PROGRAMMABLE CARD, DOUBLE LEVEL

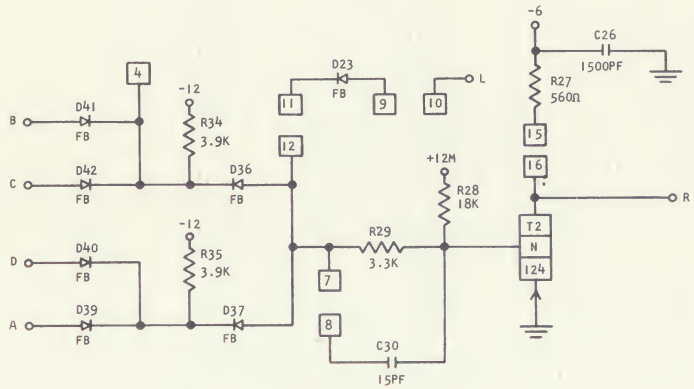
CIRCUIT NAME	CAP CODE	ASM. NO	TEST SPEC	CARD CODE
2-2 WAY, 2/CARD (-A,-0)	KT	372201	870201	AXB-
1-2 WAY, 1-3 WAY 2/CARD (-A,-0)	KU	372202	870201	AXC-
1-2 WAY, 1-3 WAY (-A,-0) WO/LOAD	KV	372208	870201	AXJ-
2 DBL 2(2W-A)-OR EXT	KW	372204	870201	AXE-
2 DBL 2(2W-A)-OR EXT WO/LOAD	KX	372210	870201	AXL-
1-3 WAY, 1-2 WAY(-A-0)WO/LOAD H.S.	KY	372531	870529	CEY-
1-3 WAY, 1-2 WAY(-A-0)W/LOAD H.S.	KZ	372530	870529	CEX-

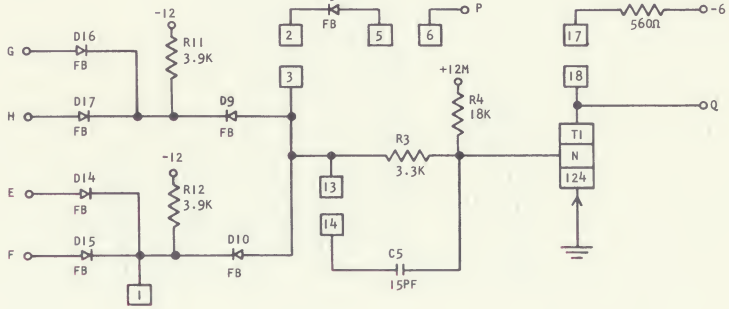
CAP CONFIGURATION





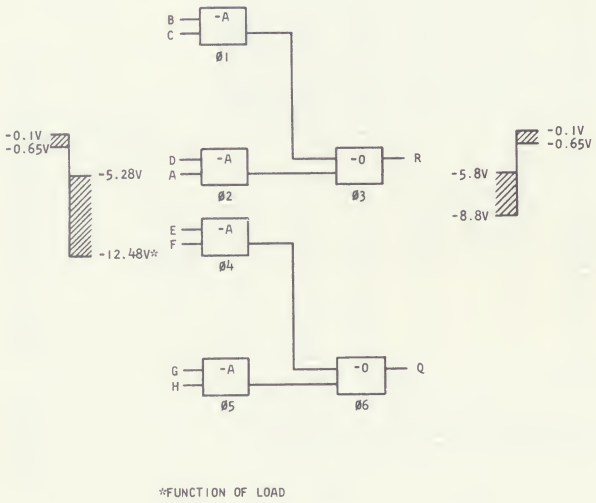
COMPONENT SIDE



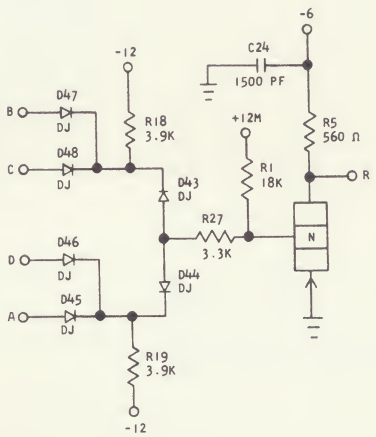


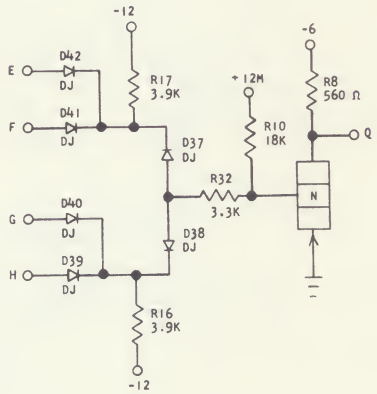
2-Two Input NAND into 1-Two Input NOR Gate (DLLB #2 or 2A)

AXB-
Ref. Eng. Spec. 870201



*FUNCTION OF LOAD





OTHER DESIGNATIONS:

CONF. 1,2,4,5 +0
CONF. 3,6 +A,-00,+AA

SEQUENCE OF OPERATION

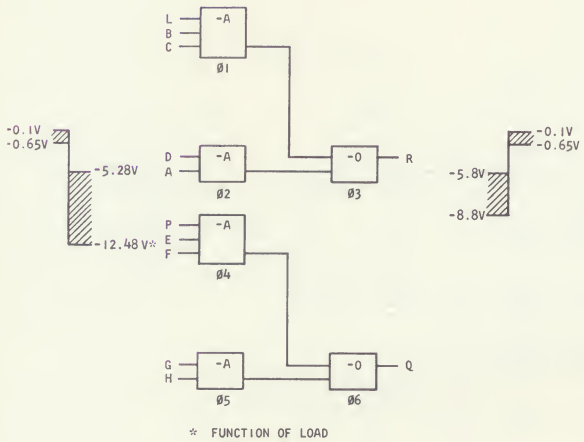
1. PINS B AND C MUST BE DOWN TO HAVE A DOWN LEVEL AT D43.
2. PINS A AND D MUST BE DOWN TO HAVE A DOWN LEVEL AT D44.
3. EITHER LEVEL DOWN AT D43 OR D44 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER B OR C UP WILL CAUSE AN UP LEVEL AT D43.
5. EITHER D OR A UP WILL CAUSE AN UP LEVEL AT D44.
6. BOTH LEVELS AT D43 AND D44 MUST BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

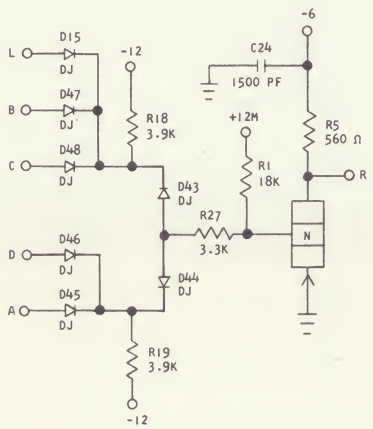
DELAY

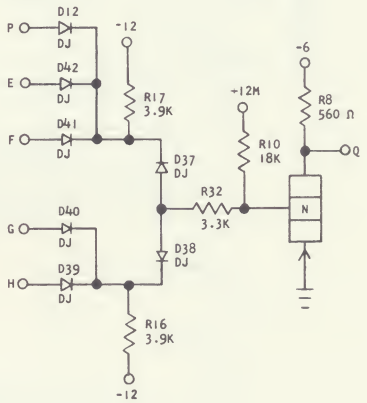
	MIN	MAX
TURN ON (NSEC)	70	240
TURN OFF (NSEC)	110	515

1-Two Input NAND and 1-Three Input NAND into Two Input NOR Gates, with load, 1.s. (DLLB #2 or 2A)

AXC-
Ref. Eng. Spec. 870201







OTHER DESIGNATIONS:

CONF. 1,2,4,5 +O
CONF. 3,6 +A,-OO,+AA,-OA,+AO

SEQUENCE OF OPERATION

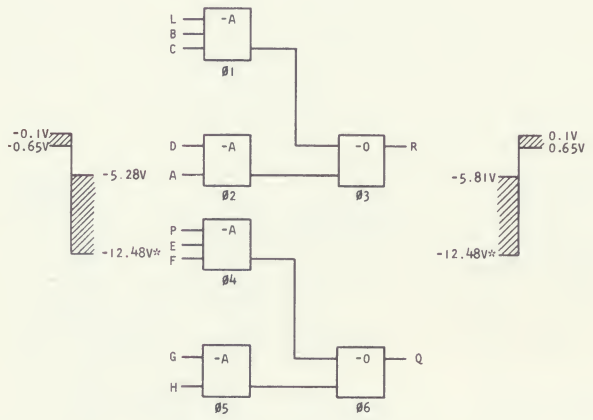
1. PINS L, B AND C MUST BE DOWN TO HAVE A DOWN LEVEL AT D43.
2. PINS A AND D MUST BE DOWN TO HAVE A DOWN LEVEL AT D44.
3. EITHER DOWN LEVEL AT D43 OR D44 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER L,B OR C UP WILL CAUSE AN UP LEVEL AT D43.
5. EITHER D OR A UP WILL CAUSE AN UP LEVEL AT D44.
6. BOTH LEVELS AT D43 AND D44 MUST BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

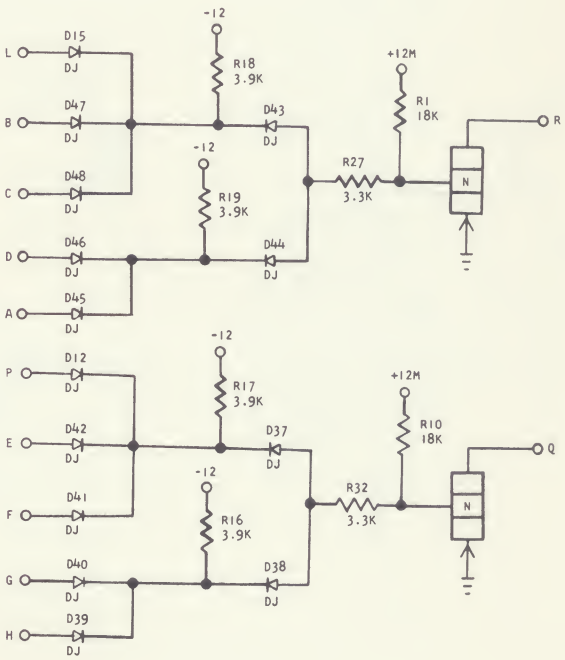
	MIN	MAX
TURN ON (NSEC)	70	240
TURN OFF (NSEC)	110	515

1-Two Input NAND and 1-Three Input NAND into Two Input NOR Gates, without load, 1.s. (DLLB #2 or 2A) Ref. Eng. Spec. 870201

AXJ-



*FUNCTION OF LOAD



OTHER DESIGNATIONS:

CONF. 1,2,4,5 +0
CONF. 3,6 +A,-00,+AA,-0A,+A0

SEQUENCE OF OPERATION

1. PINS L,B, AND C MUST BE DOWN TO HAVE A DOWN LEVEL AT D43.
2. PINS A AND D MUST BE DOWN TO HAVE A DOWN LEVEL AT D44.
3. EITHER LEVEL DOWN AT D43 OR D44 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT TO BE UP.
4. EITHER L OR B OR C UP WILL CAUSE AN UP LEVEL AT D43.
5. EITHER D OR A UP WILL CAUSE AN UP LEVEL AT D44.
6. BOTH LEVELS AT D43 AND D44 MUST BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

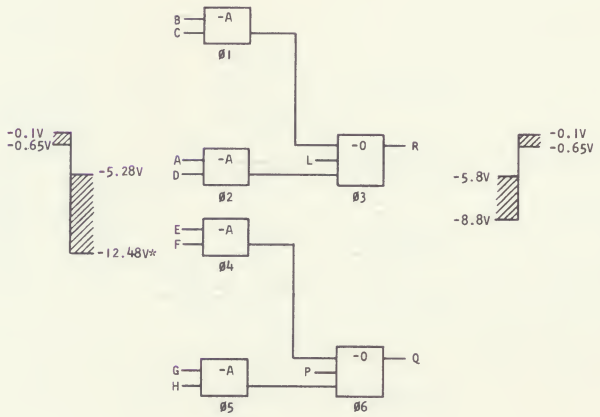
	MIN	MAX
TURN ON (NSEC)	70	240*
TURN OFF (NSEC)	110	515**

*THIS DELAY CAN INCREASE TO 280 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

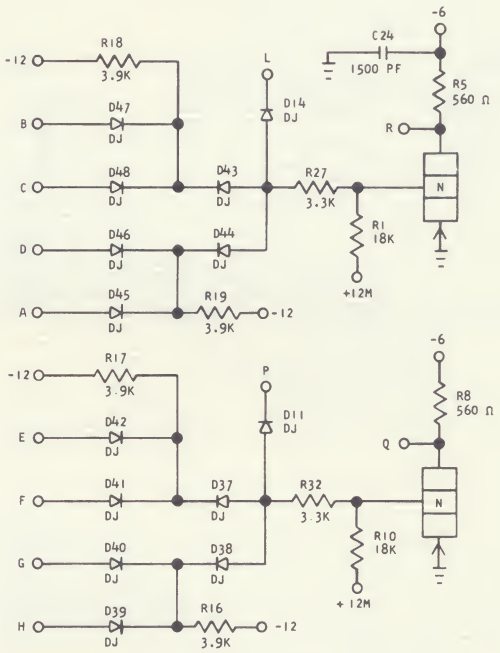
**THIS DELAY CAN INCREASE TO 570 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

2-Two Input NAND into Three Input NOR, without load, l.s. (DLLB #2 or 2A)

AXE-
Ref. Eng. Spec. 870201



*FUNCTION OF LOAD



OTHER DESIGNATIONS:

CONF. 1,2,4,5 +O
CONF. 3,6 +A,-OO,+AA,-OA,+AO

SEQUENCE OF OPERATION

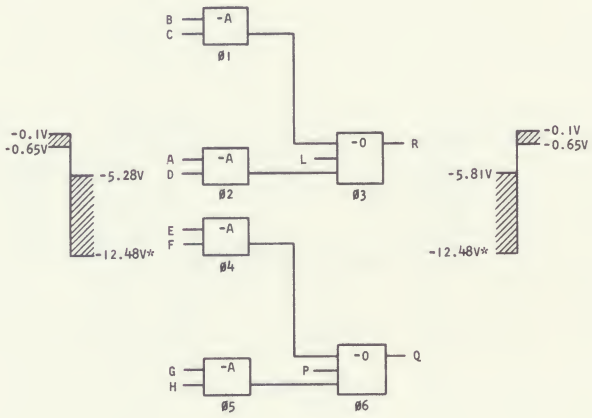
1. PINS B AND C MUST BE DOWN TO HAVE A DOWN LEVEL AT D43.
2. PINS A AND D MUST BE DOWN TO HAVE A DOWN LEVEL AT D44.
3. A DOWN LEVEL AT D14, D43 OR D44 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER B OR C UP WILL CAUSE AN UP LEVEL AT D43.
5. EITHER A OR D UP WILL CAUSE AN UP LEVEL AT D44.
6. THE LEVELS AT D14, D43 AND D44 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

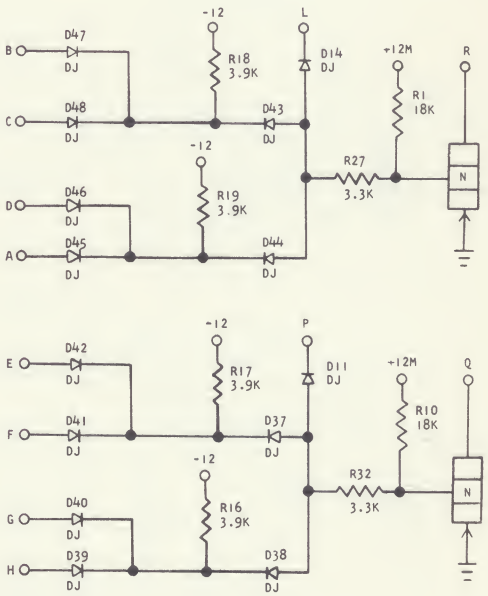
	MIN	MAX
TURN ON (NSEC)	70	240
TURN OFF (NSEC)	110	515

2-Two Input NAND into Three Input NOR,with load, l.s. (DLLB #2 or 2A)

AXL-
Ref. Eng. Spec. 870201



*FUNCTION OF LOAD



OTHER DESIGNATIONS:

CONF. 1,2,4,5 +O
CONF. 3,6 +A,-OO,+AA,-OA,+AO

SEQUENCE OF OPERATION

1. PINS B AND C MUST BE DOWN TO HAVE A DOWN LEVEL AT D43.
2. PINS A AND D MUST BE DOWN TO HAVE A DOWN LEVEL AT D44.
3. A DOWN LEVEL ON D14 OR D43 OR D44 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER B OR C UP WILL CAUSE AN UP LEVEL AT D43.
5. EITHER A OR D UP WILL CAUSE AN UP LEVEL AT D44.
6. THE LEVELS AT D43, D44 AND D14 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

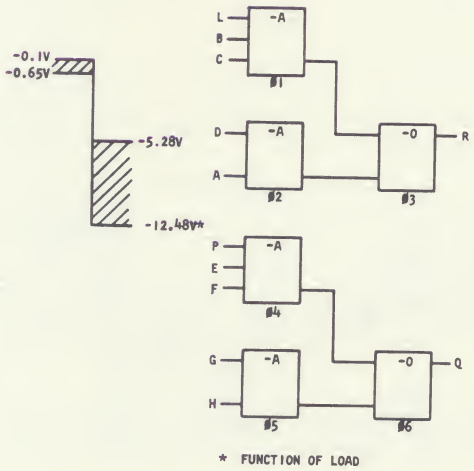
	MIN	MAX
TURN ON (NSEC)	70	240*
TURN OFF (NSEC)	110	515**

*THIS DELAY CAN INCREASE TO 280 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

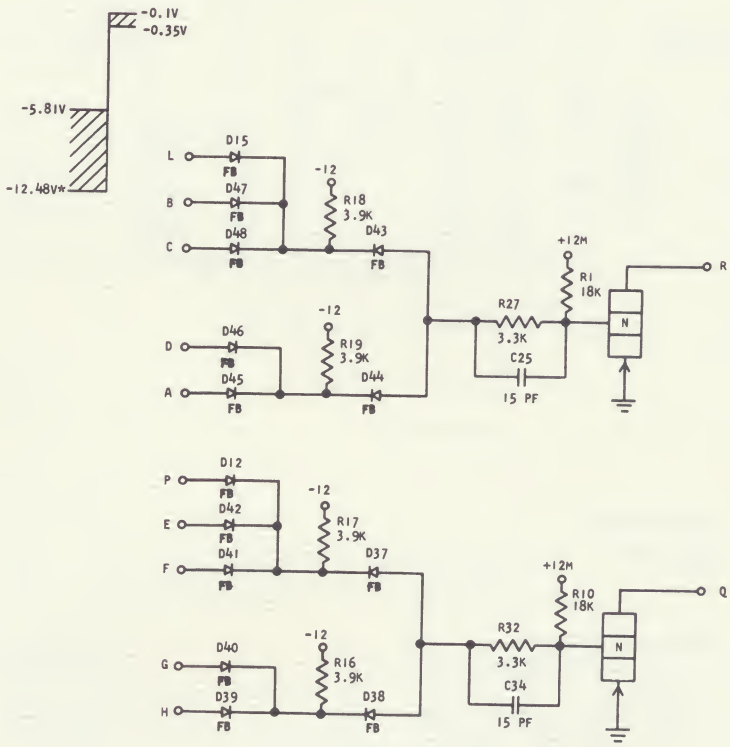
**THIS DELAY CAN INCREASE TO 570 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

2-Three Input and 1-Two Input NAND with Two Input NOR Gates, without load, h.s. (DLLB #2 or 2A)

CEY-
Ref. Eng. Spec. 870529



* FUNCTION OF LOAD



OTHER DESIGNATIONS

CONF. 1, 2, 4, 5	+O
CONF. 3, 6	+A, -OO, +AA, -OA, +AO

SEQUENCE OF OPERATION

1. PINS L, B AND C MUST BE DOWN TO HAVE A DOWN LEVEL AT D43.
2. PINS A AND D MUST BE DOWN TO HAVE A DOWN LEVEL AT D44.
3. EITHER LEVEL DOWN AT D43 OR D44 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT TO BE UP.
4. EITHER L OR B OR C UP WILL CAUSE AN UP LEVEL AT D43.
5. EITHER D OR A UP WILL CAUSE AN UP LEVEL AT D44.
6. BOTH LEVELS AT D43 AND D44 MUST BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

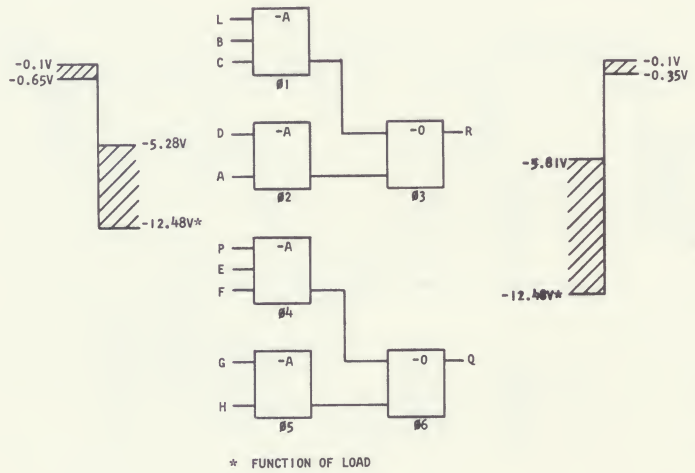
DELAY

WITH 560Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

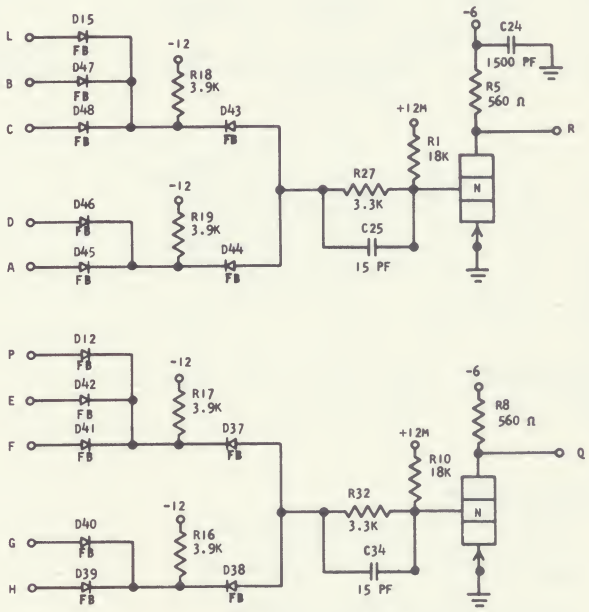
	MIN	MAX
TURN ON (NSEC)	15	280
TURN OFF (NSEC)	24	300

2-Three Input and 1-Two Input NAND with Two Input NOR Gates, with load, h.s. (DLLB #2 or 2A)

CEX-
Ref. Eng. Spec. 870529



* FUNCTION OF LOAD



OTHER DESIGNATIONS

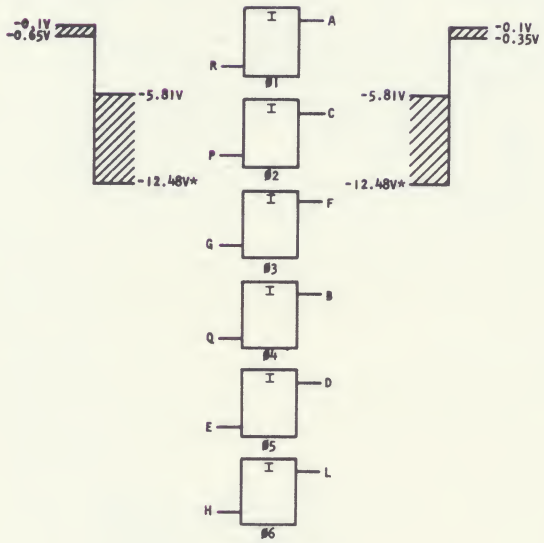
CONF. 1, 2, 4, 5	+O
CONF. 3, 6	+A, -OO, +AA, -OA, +AO

SEQUENCE OF OPERATION

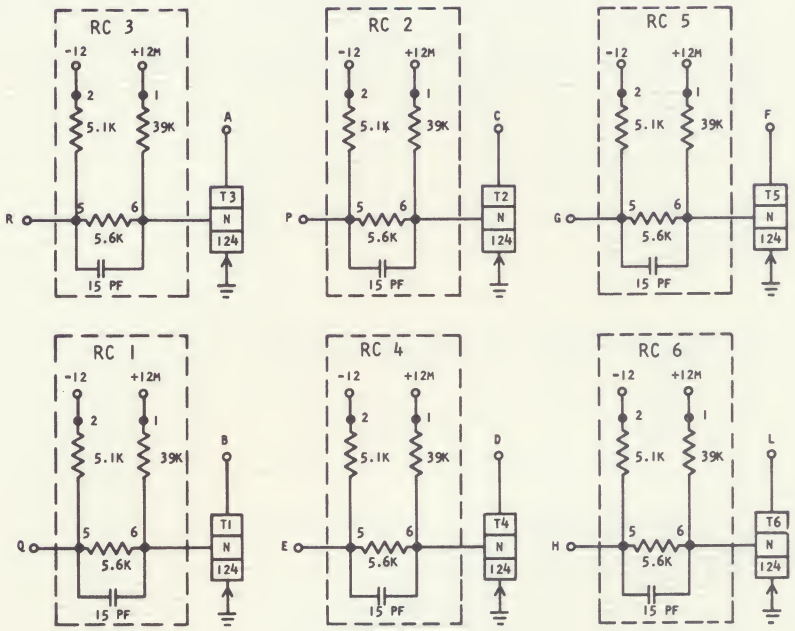
1. PINS L, B AND C MUST BE DOWN TO HAVE A DOWN LEVEL AT D43.
2. PINS A AND D MUST BE DOWN TO HAVE A DOWN LEVEL AT D44.
3. EITHER DOWN LEVEL AT D43 OR D44 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER L, B OR C UP WILL CAUSE AN UP LEVEL AT D43.
5. EITHER D OR A UP WILL CAUSE AN UP LEVEL AT D44.
6. BOTH LEVELS AT D43 AND D44 MUST BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	15	280
TURN OFF (NSEC)	24	300



* FUNCTION OF LOAD



OTHER DESIGNATIONS

ID, IA

SEQUENCE OF OPERATION

1. INPUT DOWN: TRANSISTOR ON, OUTPUT UP.
2. INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

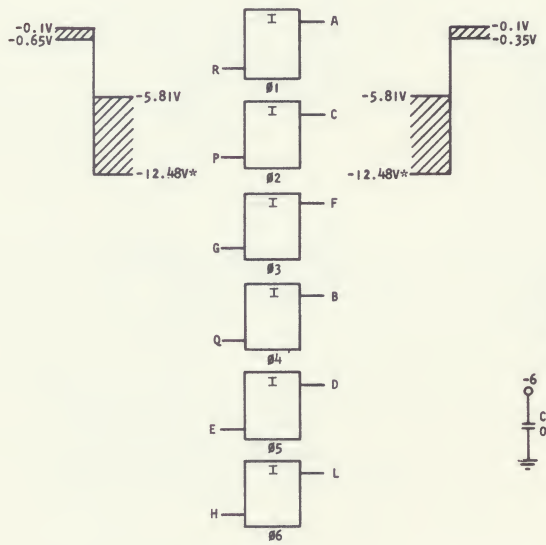
DELAY

WITH 560Ω OR 1.6K COLLECTOR RESISTOR

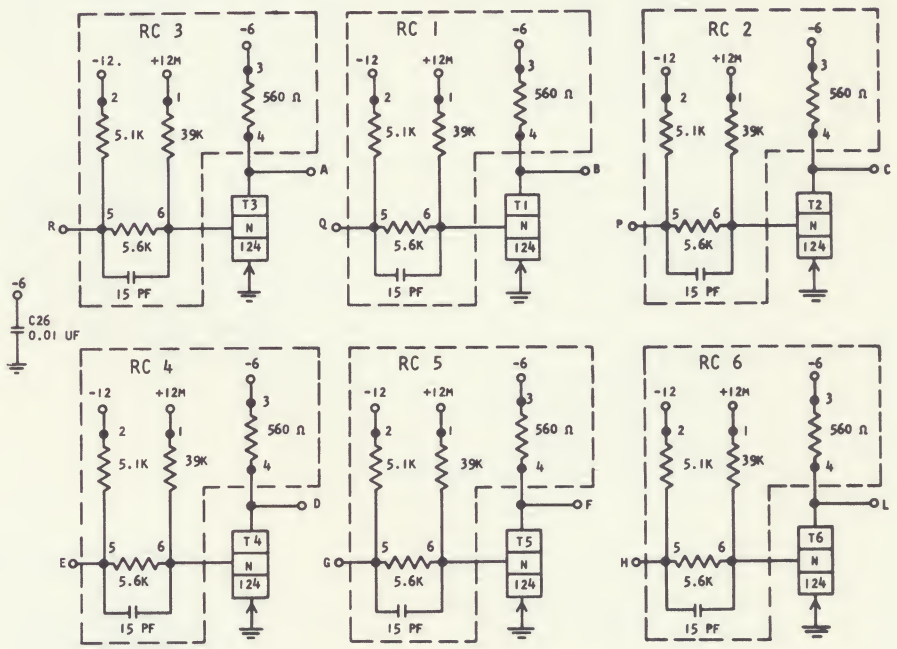
	MIN	MAX
TURN ON (NSEC)	18	100*
TURN OFF (NSEC)	15	150**

* THIS DELAY CAN INCREASE TO 180 NSEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.
** THIS DELAY CAN INCREASE TO 200 NSEC WITH A 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

6-Inverters, without load, h.s. (SLLB #1)



* FUNCTION OF LOAD



OTHER DESIGNATIONS

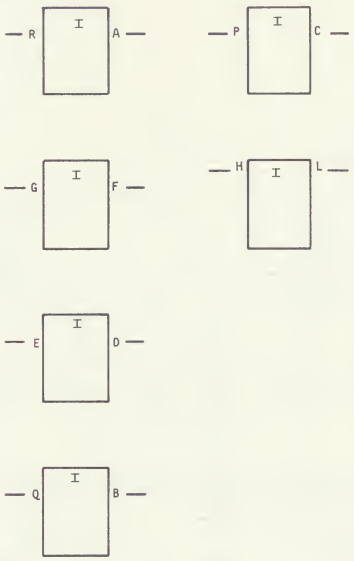
ID, IA

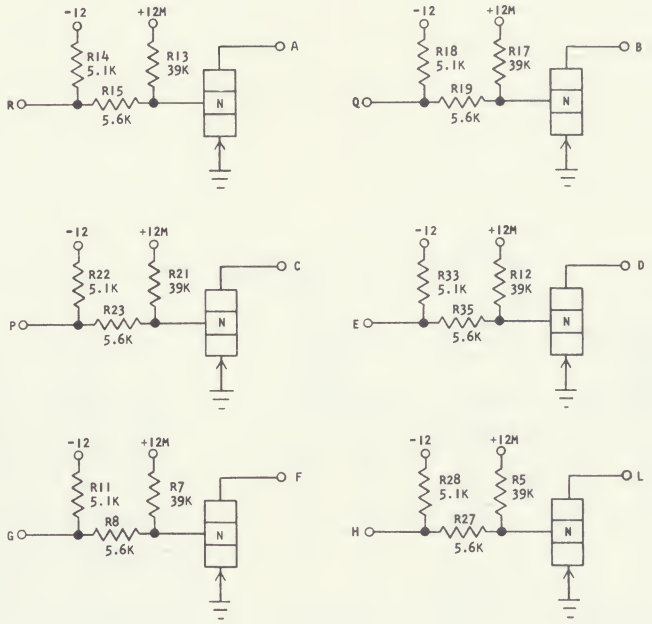
SEQUENCE OF OPERATION

1. INPUT DOWN: TRANSISTOR ON, OUTPUT UP.
2. INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	18	100
TURN OFF (NSEC)	15	150





SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. ALL COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
R,Q,P, E,G,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
A,B,C, D,F,L	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY: SDTDL - LOW SPEED

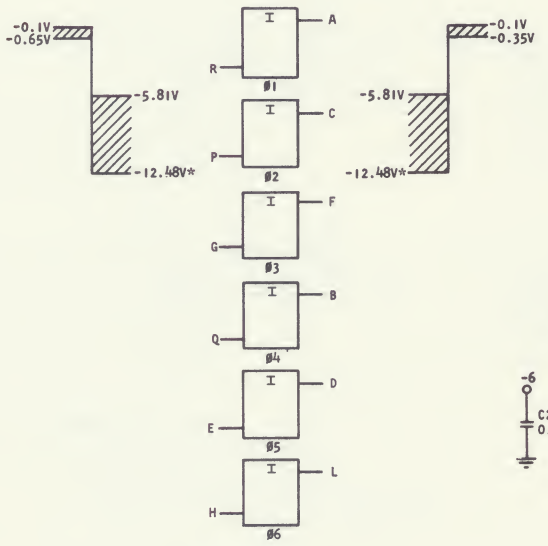
LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

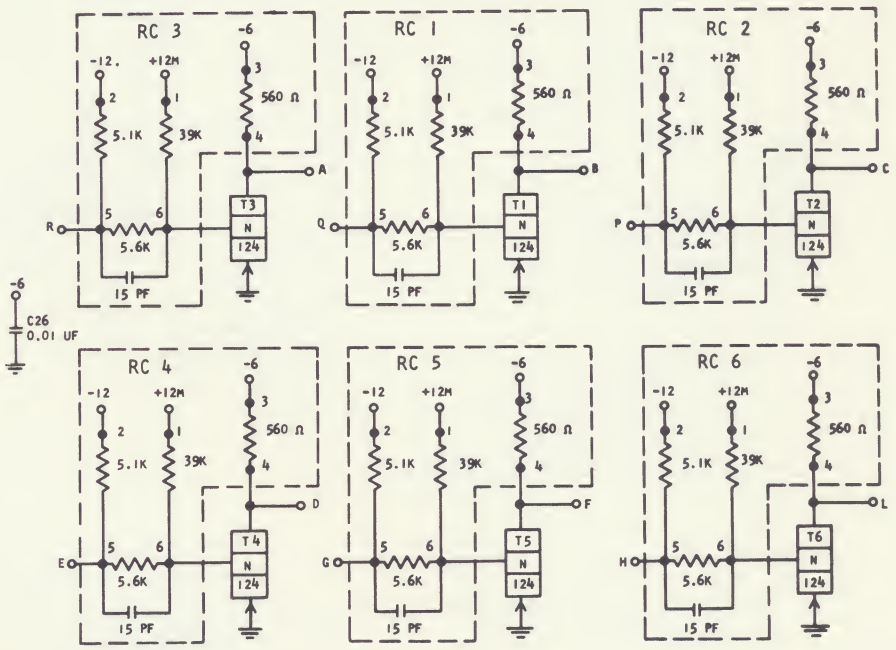
*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

6-Inverters, without load, h.s. (SLLB #1)



* FUNCTION OF LOAD



OTHER DESIGNATIONS

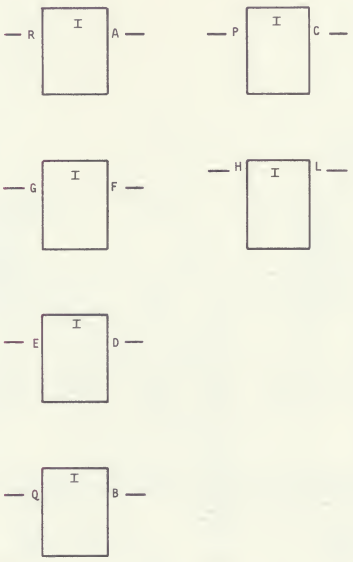
ID, IA

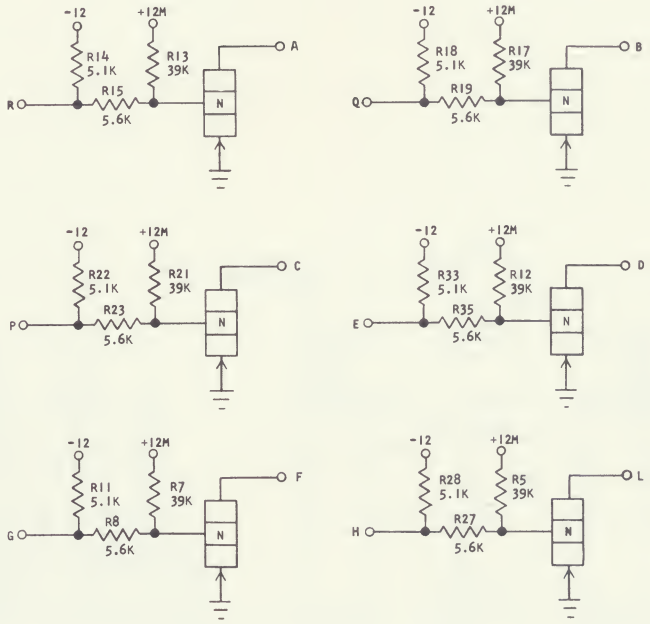
SEQUENCE OF OPERATION

1. INPUT DOWN: TRANSISTOR ON, OUTPUT UP.
2. INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	18	100
TURN OFF (NSEC)	15	150





SEQUENCE OF OPERATION

1. INPUT DOWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN
3. ALL COLLECTORS MUST BE LOADED
4. LOGIC BLOCKS MAY HAVE SYMBOLS OTHER THAN SHOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
R,Q,P, E,G,H	Y	INPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8
A,B,C, D,F,L	Y	OUTPUT		UP	-.65	-.1
				DOWN	-5.81	-8.8

DELAY: SDTDL - LOW SPEED

LOGIC BLOCK WITH 560 OHM COLLECTOR RESISTOR

	MIN.	MAX.
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

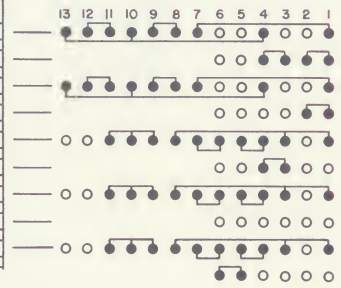
**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

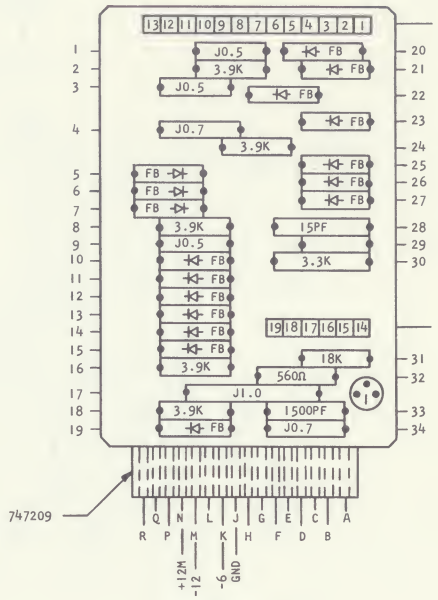
PROGRAMMABLE CARD, DOUBLE LEVEL

P/N 370954
5Y**

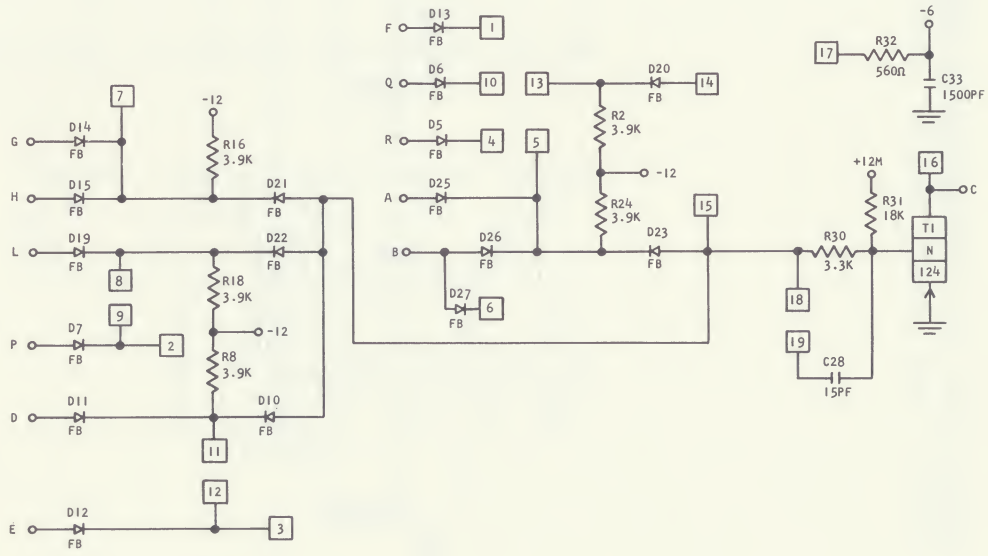
CIRCUIT NAME	CAP CODE	ASM. NO	TEST SPEC	CARD CODE
4-2 WAY, 1-3 WAY (-A,-0)	KN	372207	870201	AXH-
4-2 WAY, 1-3 WAY (-A,-0) WO/LOAD	KP	372213	870201	AXP-
4-3 WAY (-A,-0) W/LOAD - SDTDL	KQ	372214	870201	AXQ-
4-3 WAY (-A,-0) WO/LOAD - SDTDL	KR	372236	870201	AXW-
4-3 WAY (-A,-0) WO/LOAD H.S.	KS	372527	870529	DKX-

CAP CONFIGURATION



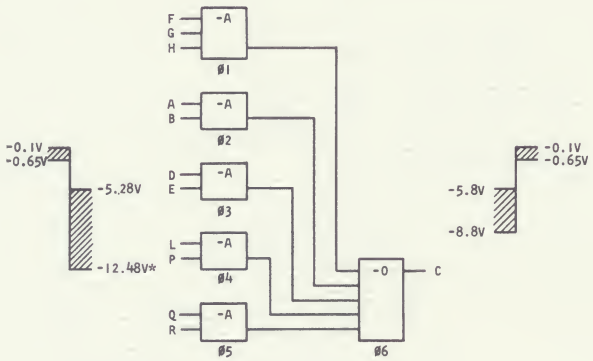


COMPONENT SIDE

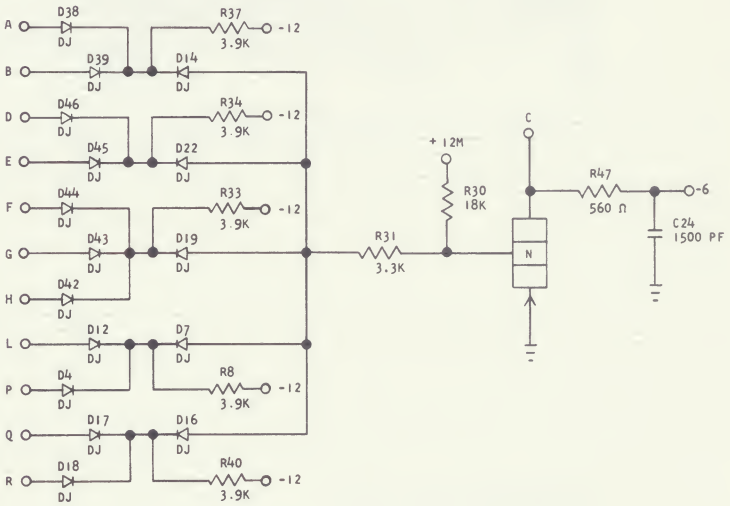


4-Two Input and 1-Three Input NAND into Five Input NOR Gates, with load, l.s. (DLLB #2 or 2A)

AXH-
Ref. Eng. Spec. 870201



*FUNCTION OF LOAD



OTHER DESIGNATIONS:

CONF. 1-5 +0
CONF. 6 +A,-00,+AA,-0A,+A0

SEQUENCE OF OPERATION

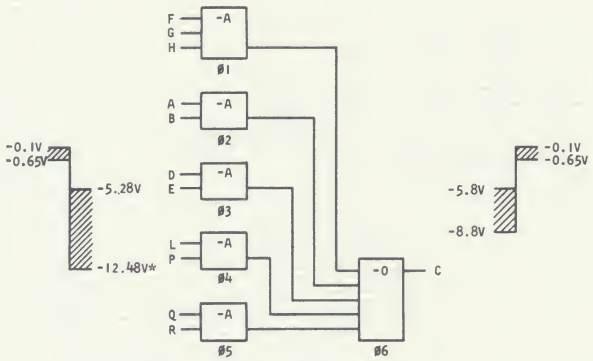
1. PINS A AND B MUST BE DOWN TO HAVE A DOWN LEVEL AT D14.
2. PINS F,G AND H MUST BE DOWN TO HAVE A DOWN LEVEL AT D19.
3. A DOWN LEVEL AT D7 OR D14 OR D16 OR D19 OR D22 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER A OR B UP WILL CAUSE AN UP LEVEL AT D14.
5. EITHER F OR G OR H UP WILL CAUSE AN UP LEVEL AT D19.
6. THE LEVELS AT D14,D22,D19,D7 AND D16 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

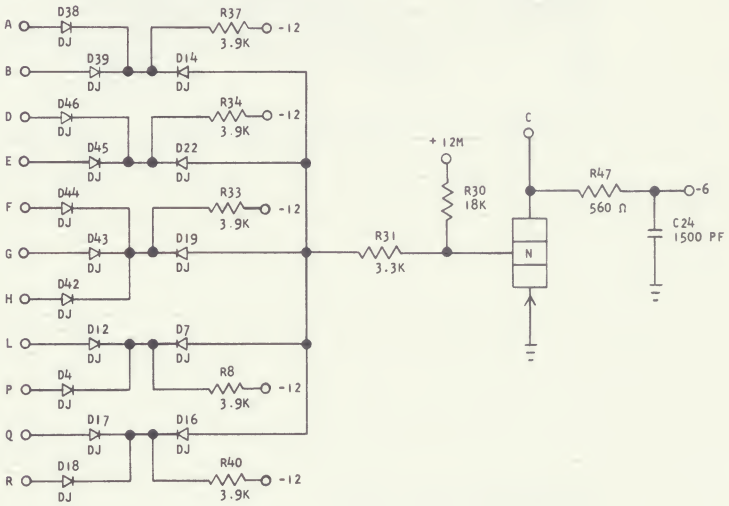
	MIN	MAX
TURN ON (NSEC)	70	240
TURN OFF (NSEC)	110	515

4-Two Input and 1-Three Input NAND into Five Input NOR Gates, with load, l.s. (DLLB #2 or 2A)

AXH-
Ref. Eng. Spec. 870201



*FUNCTION OF LOAD



OTHER DESIGNATIONS:

CONF. 1-5 +0
CONF. 6 +A,-00,+AA,-0A,+A0

SEQUENCE OF OPERATION

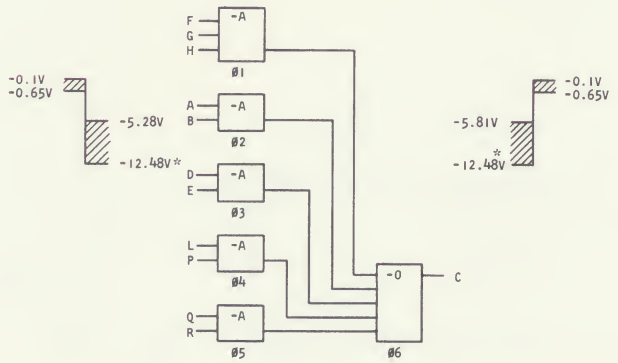
1. PINS A AND B MUST BE DOWN TO HAVE A DOWN LEVEL AT D14.
2. PINS F,G AND H MUST BE DOWN TO HAVE A DOWN LEVEL AT D19.
3. A DOWN LEVEL AT D7 OR D14 OR D16 OR D19 OR D22 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER A OR B UP WILL CAUSE AN UP LEVEL AT D14.
5. EITHER F OR G OR H UP WILL CAUSE AN UP LEVEL AT D19.
6. THE LEVELS AT D14,D22,D19,D7 AND D16 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

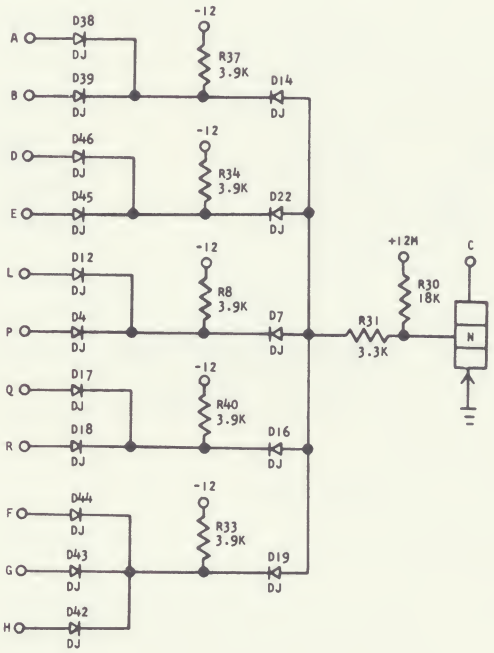
DELAY

	MIN	MAX
TURN ON (NSEC)	70	240
TURN OFF (NSEC)	110	515

4-Two Input and 1-Three Input NAND into Five Input NOR Gates, without load, l.s. (DLLB #2 or 2A)

AXP-
Ref. Eng. Spec. 870201





OTHER DESIGNATIONS:

CONF. 1-5 +0
CONF. 6 +A, -00, +AA, -0A, +A0

SEQUENCE OF OPERATION

1. PINS A AND B MUST BE DOWN TO HAVE A DOWN LEVEL AT D14.
2. PINS F,G AND H MUST BE DOWN TO HAVE A DOWN LEVEL AT D19.
3. A DOWN LEVEL AT D7, D14, D16, D19 OR D22 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER A OR B UP WILL CAUSE AN UP LEVEL AT D14.
5. EITHER F,G OR H UP WILL CAUSE AN UP LEVEL AT D19.
6. THE LEVELS AT D7, D14, D16, D19 AND D22 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

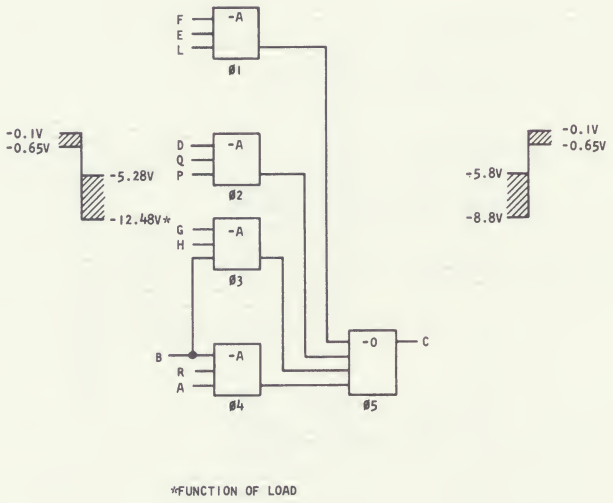
	MIN	MAX
TURN ON (NSEC)	70	240*
TURN OFF (NSEC)	110	515**

*THIS DELAY CAN INCREASE TO 280 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

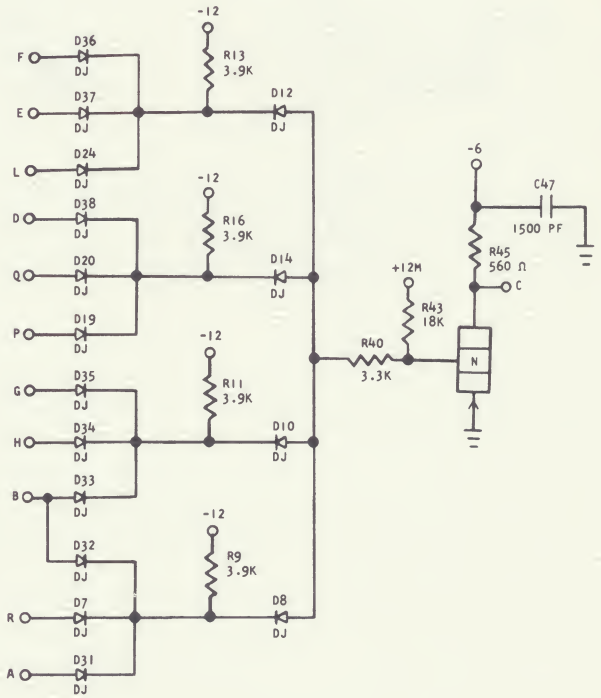
**THIS DELAY CAN INCREASE TO 570 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

4-Three Input NAND into Five Input NOR Gates, with load, l.s. (DLLB #2 or 2A)

AXQ-
Ref. Eng. Spec. 870201



*FUNCTION OF LOAD



OTHER DESIGNATIONS:

CONF. 1-4 +0
CONF. 5 +A,-OO,+AA,-OA,+AO

SEQUENCE OF OPERATION

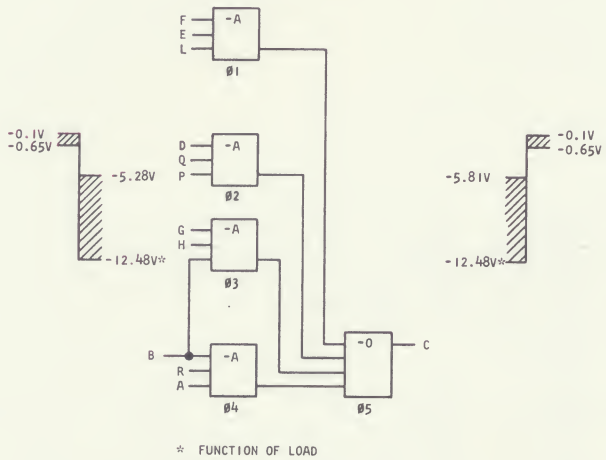
1. PINS F, E AND L MUST BE DOWN TO HAVE A DOWN LEVEL AT D12.
2. PINS D, Q AND P MUST BE DOWN TO HAVE A DOWN LEVEL AT D14.
3. A DOWN LEVEL AT D8, D10, D12 OR D14 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER F, E OR L UP WILL CAUSE AN UP LEVEL AT D12.
5. EITHER D, Q OR P UP WILL CAUSE AN UP LEVEL AT D14.
6. THE LEVELS AT D8, D10, D12 AND D14 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

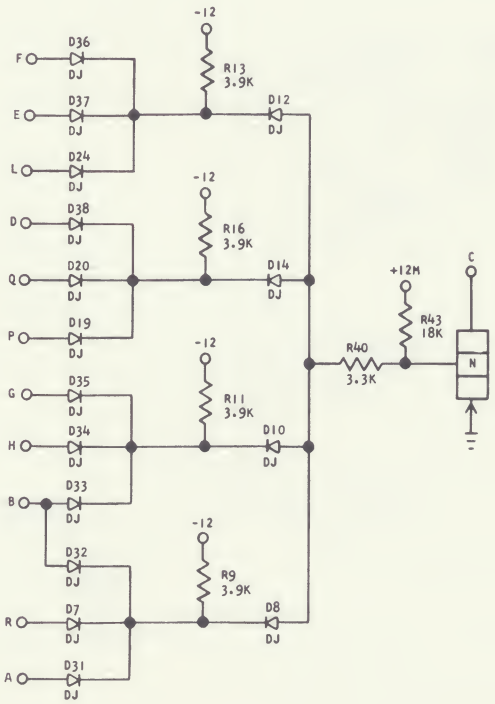
	MIN	MAX
TURN ON (NSEC)	70	240
TURN OFF (NSEC)	110	515

4-Three Input NAND into Five Input NOR Gates, without load, l.s. (DLLB #2 or 2A)

AXW-
Ref. Eng. Spec. 870201



* FUNCTION OF LOAD



OTHER DESIGNATIONS:

CONF. 1-4 +0
CONF. 5 +A,-OO,+AA,-OA,+AO

SEQUENCE OF OPERATION

1. PINS F,E AND L MUST BE DOWN TO HAVE A DOWN LEVEL AT D12.
2. PINS D,Q AND P MUST BE DOWN TO HAVE A DOWN LEVEL AT D14.
3. A DOWN LEVEL AT D8, D10, D12 OR D14 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER F,E OR L UP WILL CAUSE AN UP LEVEL AT D12.
5. EITHER D,Q OR P UP WILL CAUSE AN UP LEVEL AT D14.
6. THE LEVELS AT D8, D10, D12 AND D14 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

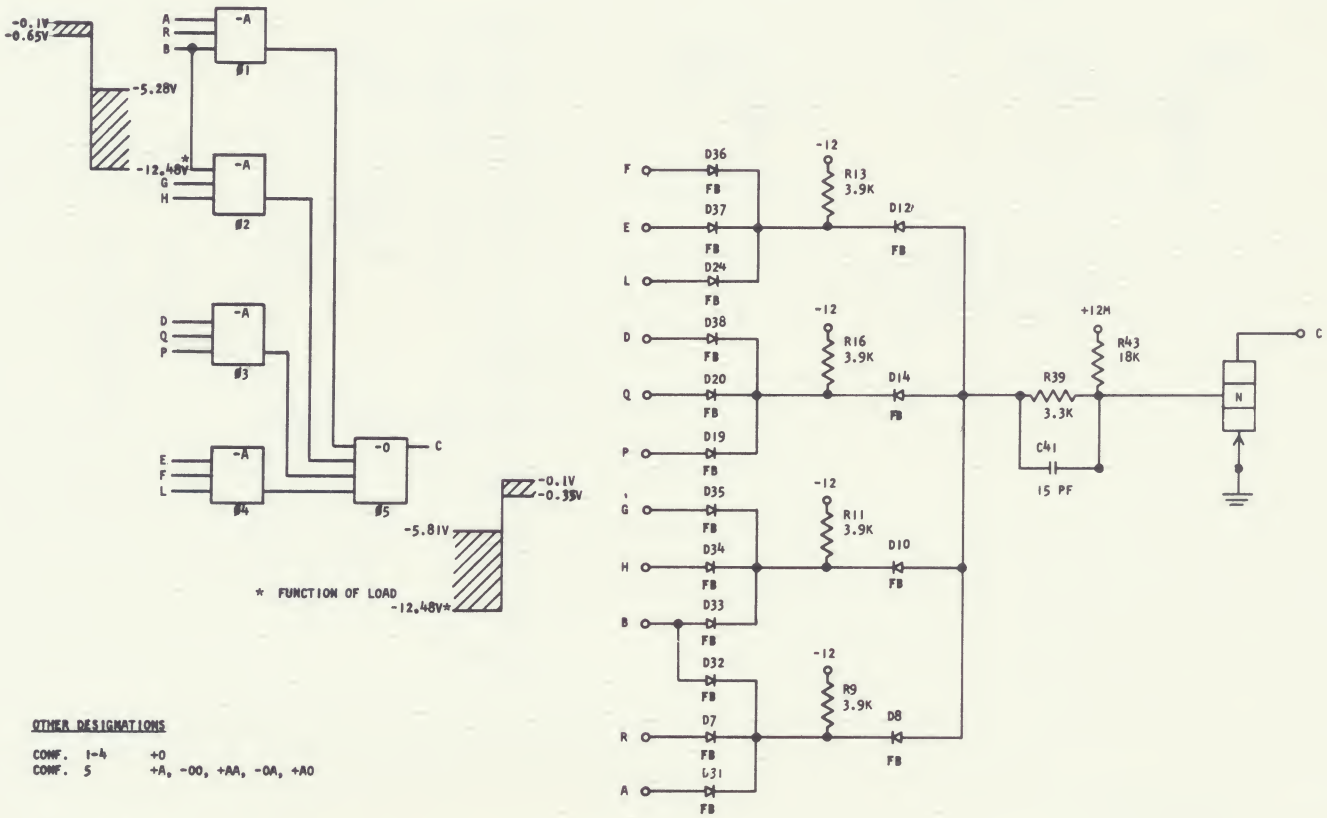
	MIN	MAX
TURN ON (NSEC)	70	240*
TURN OFF (NSEC)	110	515**

*THIS DELAY CAN INCREASE TO 280 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 570 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

4-Three Input NAND into Five Input NOR Gates,
without load, h.s. (DLLB #2 or 2A)

DKX-
Ref. Eng. Spec. 870201



OTHER DESIGNATIONS

CONF. 1-4 +0
CONF. 5 +A, -00, +AA, -0A, +A0

SEQUENCE OF OPERATION

1. PINS F, E AND L MUST BE DOWN TO HAVE A DOWN LEVEL AT D12.
2. PINS D, Q AND P MUST BE DOWN TO HAVE A DOWN LEVEL AT D14.
3. A DOWN LEVEL AT D8, D10, D12 OR D14 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER F, E OR L UP WILL CAUSE AN UP LEVEL AT D12.
5. EITHER D, Q OR P UP WILL CAUSE AN UP LEVEL AT D14.
6. THE LEVELS AT D8, D10, D12 AND D14 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

WITH 560Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

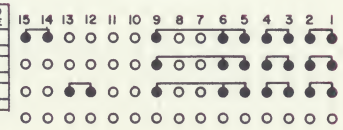
	MIN	MAX
TURN ON (NSEC)	15	280
TURN OFF (NSEC)	24	300

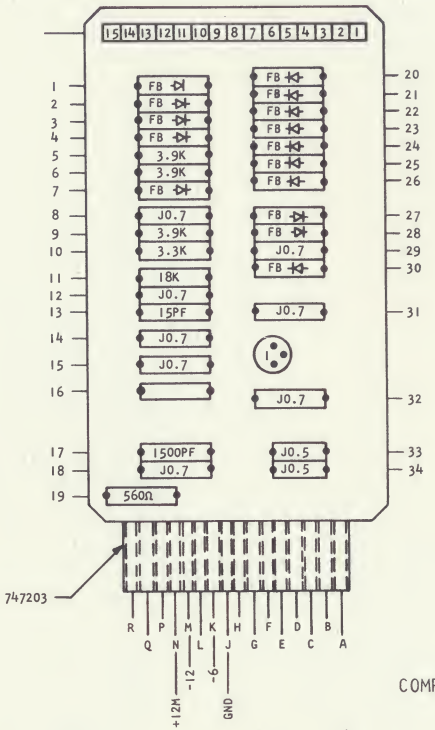
PROGRAMMABLE CARD, DOUBLE LEVEL

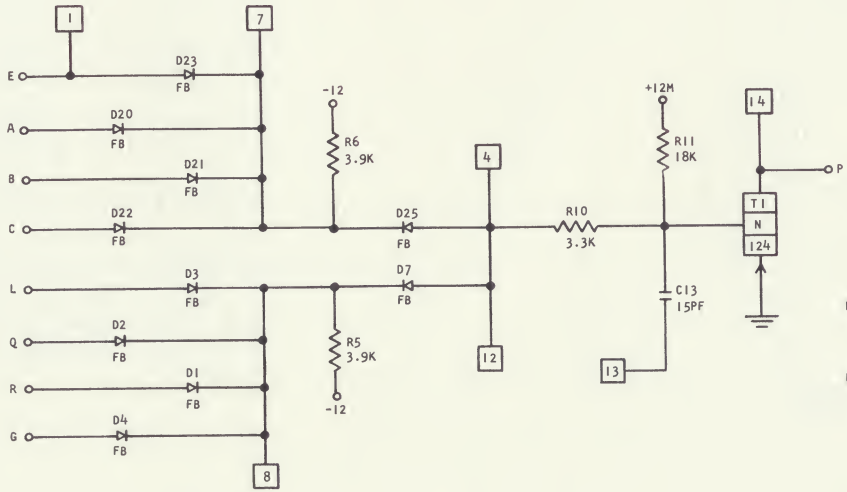
P/N 370951
1Y**

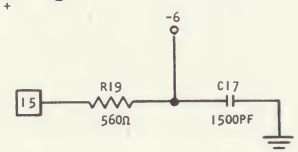
CAP CONFIGURATION

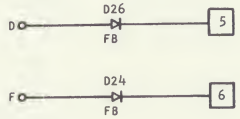
CIRCUIT NAME	CAP CODE	ASM. NO	TEST SPEC	CARD CODE
3-4 WAY LOAD (-A, -0)	JN	372206	870201	AXG-
3-4 WAY W/O LOAD (-A, -0)	JP	372212	870201	AXN-
3-4 WAY (-A, -0) W/O LOAD H.S.	JQ	372529	870529	DKZ-

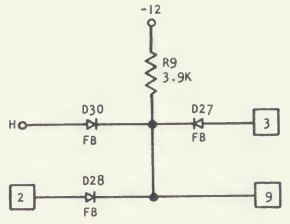






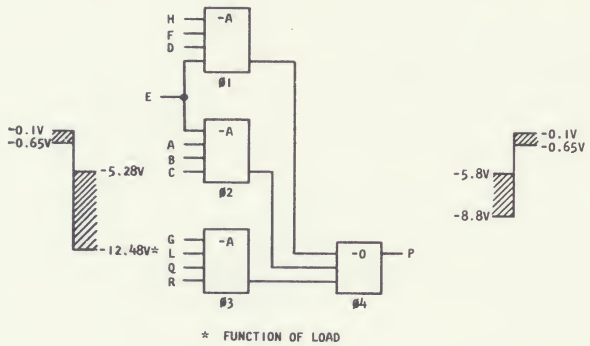




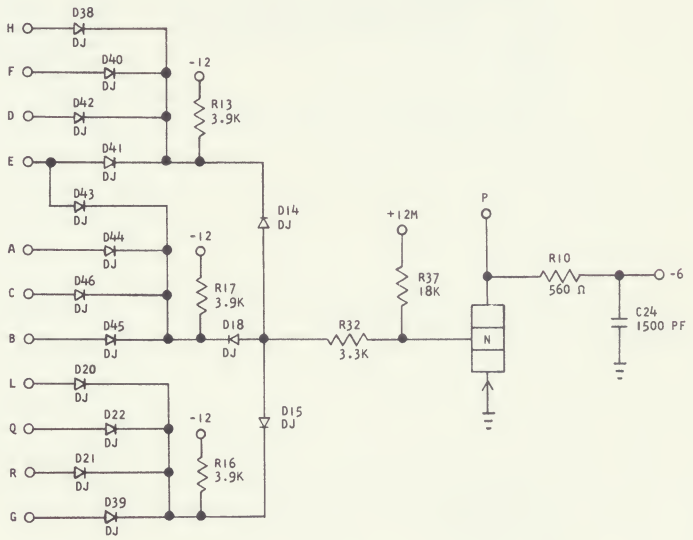


3-Four Input NAND into three Input NOR Gates, with load, l.s. (DLLB #2 or 2A)

AXG-
Ref. Eng. Spec. 870201



* FUNCTION OF LOAD



OTHER DESIGNATIONS

CONF. 1-3 +0
CONF. 4 +A,-00,+AA,-0A,+A0

SEQUENCE OF OPERATION

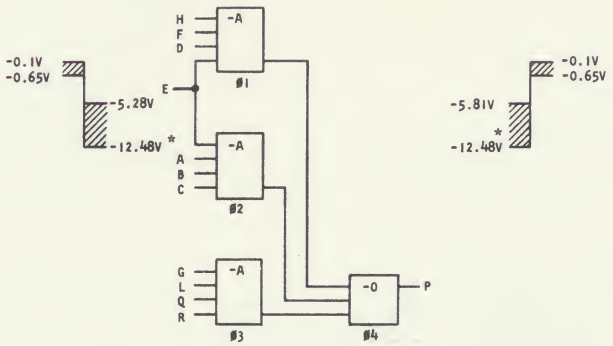
1. PINS A,B,C,E MUST BE DOWN TO HAVE A DOWN LEVEL AT D18.
2. PINS G,L,Q,R MUST BE DOWN TO HAVE A DOWN LEVEL AT D15.
3. A DOWN LEVEL AT D14, OR D15, OR D18 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER G,L,Q OR R UP WILL CAUSE AN UP LEVEL AT D15.
5. EITHER A,B,C OR E UP WILL CAUSE AN UP LEVEL AT D18.
6. THE LEVELS AT D18,D15 AND D14 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

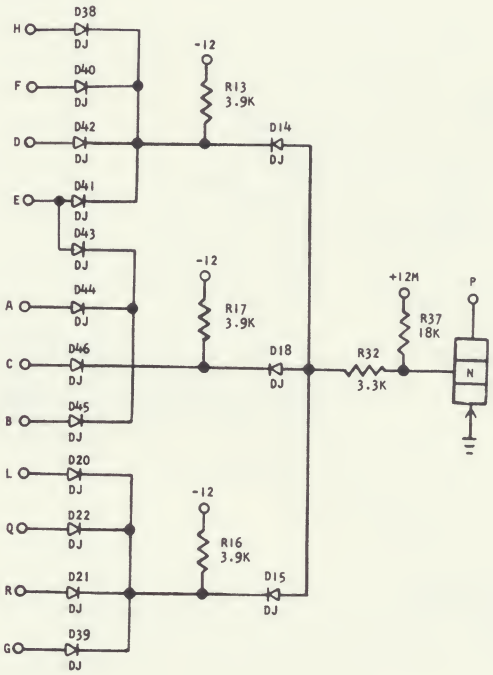
	MIN	MAX
TURN ON (NSEC)	70	240
TURN OFF (NSEC)	110	515

3-Four Input NAND into three Input NOR Gates,
without load, 1.s. (DLLB #2 or 2A)

AXN-
Ref. Eng. Spec. 870201



*FUNCTION OF LOAD



OTHER DESIGNATIONS:

CONF. 1-3 +O
CONF. 4 : +A,-OO,+AA,-OA,+AO

SEQUENCE OF OPERATION

1. PINS A,B,C AND E MUST BE DOWN TO HAVE A DOWN LEVEL AT D18.
2. PINS G,L,Q AND R MUST BE DOWN TO HAVE A DOWN LEVEL AT D15.
3. A DOWN LEVEL AT D14, D15 OR D18 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER A,B,C OR E UP WILL CAUSE AN UP LEVEL AT D18.
5. EITHER G,L,Q OR R UP WILL CAUSE AN UP LEVEL AT D15.
6. THE LEVELS AT D18, D15 AND D14 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

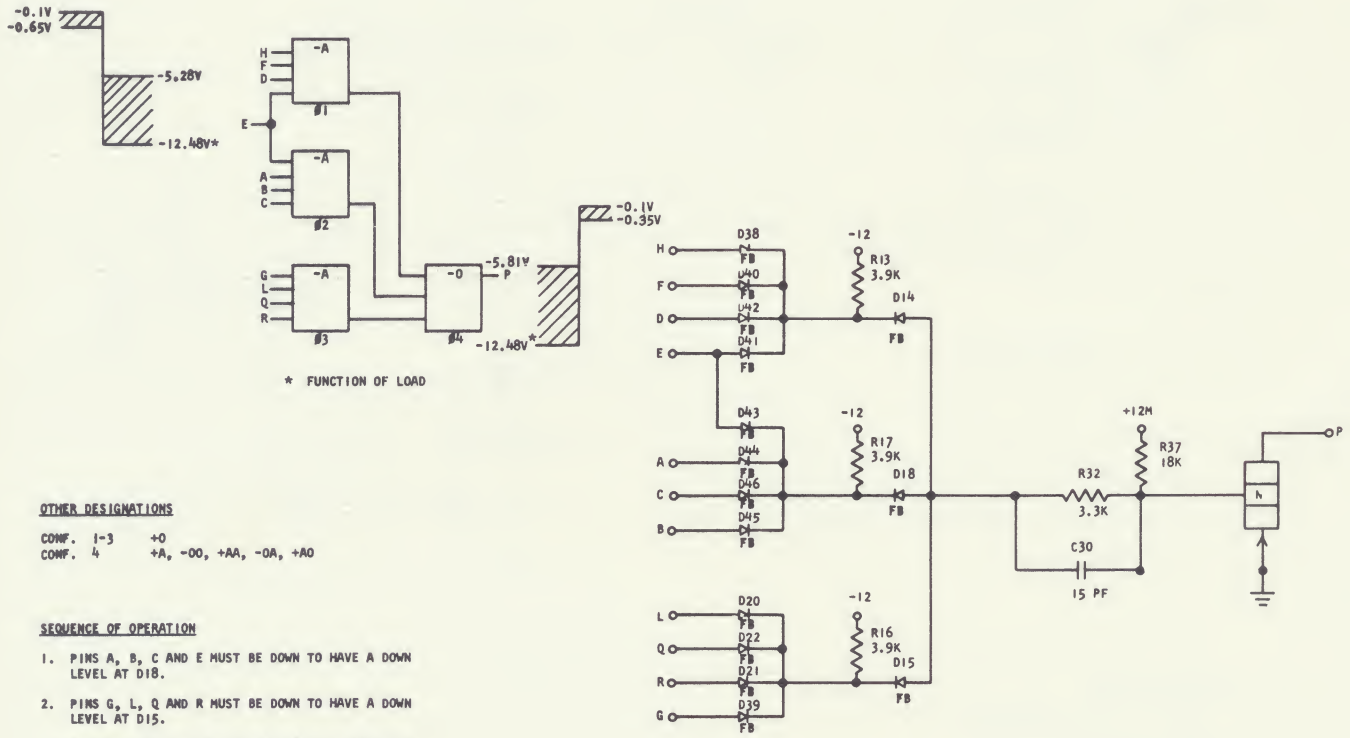
	MIN	MAX
TURN ON (NSEC)	70	240*
TURN OFF (NSEC)	110	515**

*THIS DELAY CAN INCREASE TO 280 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 570 NSEC IF THE COLLECTOR RESISTOR IS 6.2K RETURNED TO -12V.

3-Four Input NAND into three Input NOR Gates,
without load, h.s. (DLLB #2 or 2A)

DKZ-
Ref. Eng. Spec. 870529



* FUNCTION OF LOAD

OTHER DESIGNATIONS

CONF. 1-3 +O
CONF. 4 +A, -OO, +AA, -OA, +AO

SEQUENCE OF OPERATION

1. PINS A, B, C AND E MUST BE DOWN TO HAVE A DOWN LEVEL AT D18.
2. PINS G, L, Q AND R MUST BE DOWN TO HAVE A DOWN LEVEL AT D15.
3. A DOWN LEVEL AT D14, D15 OR D18 WILL CAUSE THE TRANSISTOR TO TURN ON, THE OUTPUT WILL BE UP.
4. EITHER A, B, C OR E UP WILL CAUSE AN UP LEVEL AT D18.
5. EITHER G, L, Q OR R UP WILL CAUSE AN UP LEVEL AT D15.
6. THE LEVELS AT D18, D15 AND D14 MUST ALL BE UP TO TURN THE TRANSISTOR OFF, THE OUTPUT WILL BE DOWN.

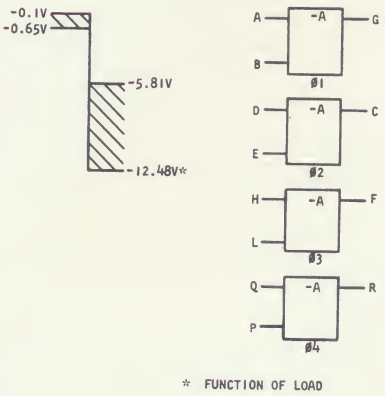
DELAY

WITH 560Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

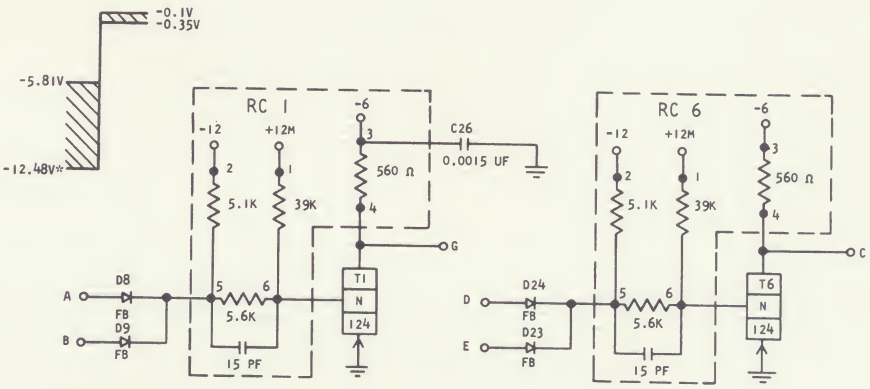
	MIN	MAX
TURN ON (NSEC)	15	280
TURN OFF (NSEC)	24	300

P/N 372585
ZGG-
Ref. Eng. Spec. 870585

4-Two Input NAND Gates, with load h.s. (SLLB #1)



* FUNCTION OF LOAD



OTHER DESIGNATIONS

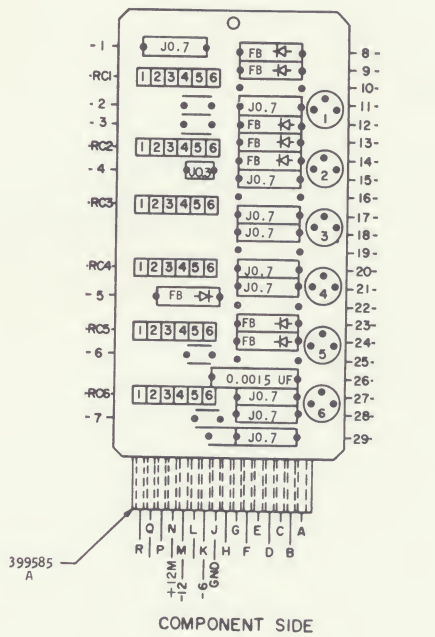
+0, -A0, +0A, +00, I, IO, IA

SEQUENCE OF OPERATION

1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

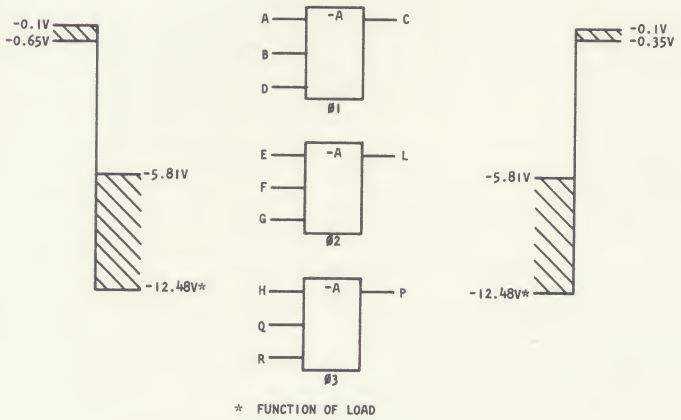
DELAY

	MIN	MAX
TURN ON (NSEC)	18	100
TURN OFF (NSEC)	15	150

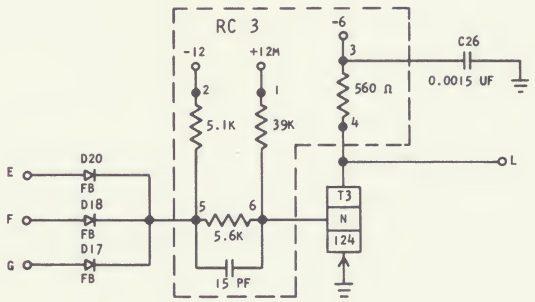


P/N 372587
ZGJ-

3-Three Input NAND Gates, with load h.s. (SLLB #1) Ref. Eng. Spec. 870585



* FUNCTION OF LOAD



OTHER DESIGNATIONS

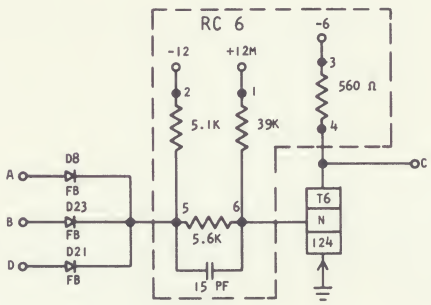
+0, -A0, +0A, +00, I, I0, IA

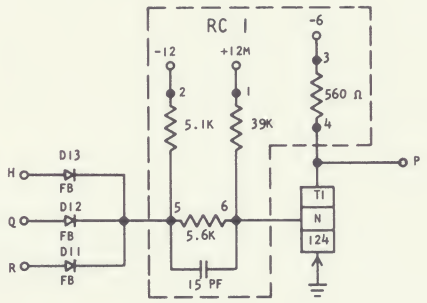
SEQUENCE OF OPERATION

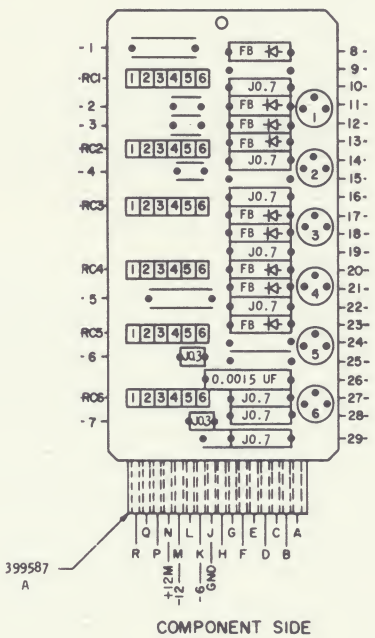
1. ALL INPUTS DOWN: TRANSISTOR ON, OUTPUT UP.
2. ANY INPUT UP: TRANSISTOR OFF, OUTPUT DOWN.

DELAY

	MIN	MAX
TURN ON (NSEC)	18	100
TURN OFF (NSEC)	15	150



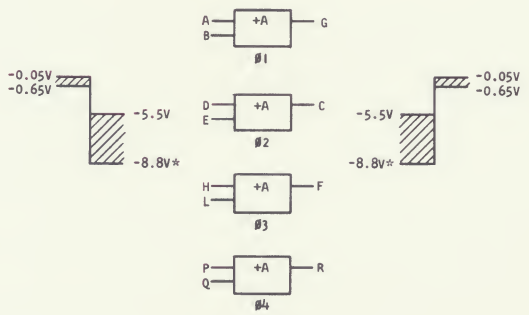




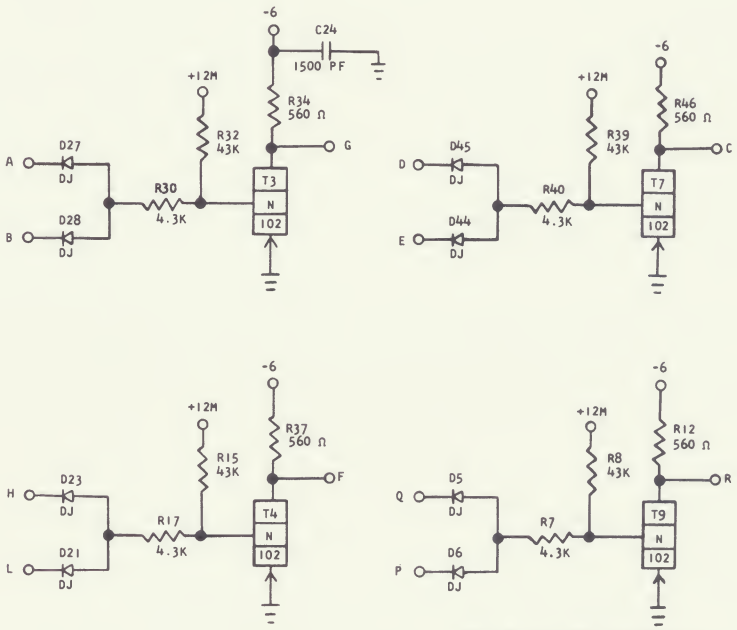
COMPONENT SIDE

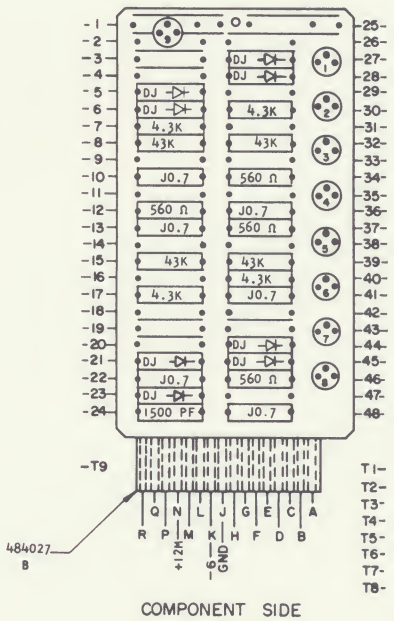
P/N 372196
DEP-

4-Two Input AND Gates, with load l.s. (SLLB #2) Ref. Eng. Spec. 870196



* FUNCTION OF LOAD





COMPONENT SIDE

OTHER DESIGNATIONS:

-0, +AO, -OA, +AA, -OO

SEQUENCE OF OPERATION

1. ALL INPUTS UP: TRANSISTOR OFF, OUTPUT DOWN.
2. ANY INPUT DOWN: TRANSISTOR ON, OUTPUT UP.

DELAY

	MIN	MAX
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

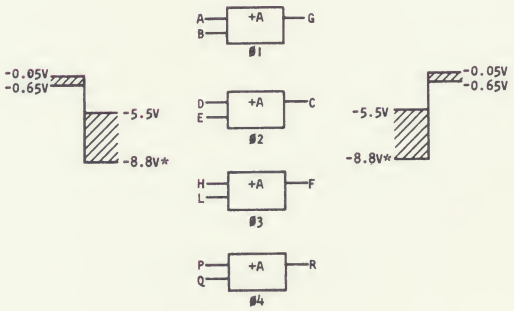
*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

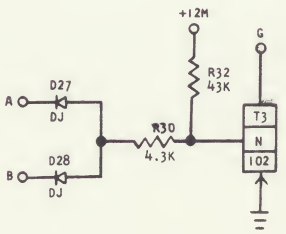
P/N 372197
AXA-

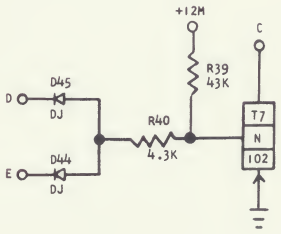
4-Two Input AND Gates,without load, l.s. (SLLB #2)

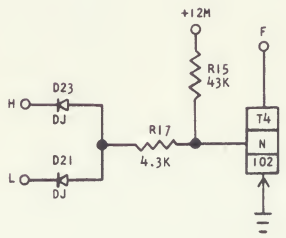
Ref. Eng. Spec. 870196

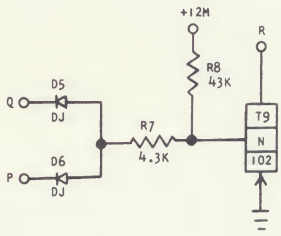


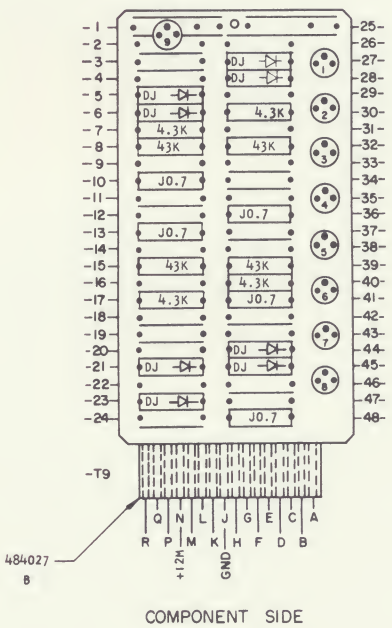
* FUNCTION OF LOAD











COMPONENT SIDE

OTHER DESIGNATIONS:

-0, +A0, -0A, +AA, -00

SEQUENCE OF OPERATION

1. ALL INPUTS UP: TRANSISTOR OFF, OUTPUT DOWN.

2. ANY INPUT DOWN: TRANSISTOR ON, OUTPUT UP.

DELAY

WITH 560 Ω, 1.6K OR 6.2K COLLECTOR RESISTOR

	MIN	MAX
TURN ON (NSEC)	75	100*
TURN OFF (NSEC)	40	200**

*THIS DELAY CAN INCREASE TO 200 NSEC WHEN THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

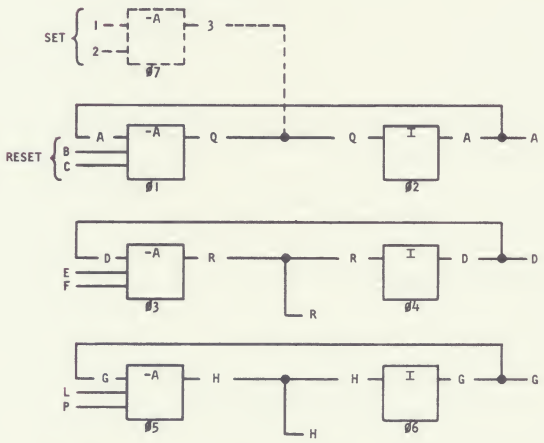
**THIS DELAY CAN INCREASE TO 350 NSEC WHEN THE DRIVING BLOCK OR THE BLOCK THAT DRIVES THE DRIVING BLOCK HAS 6.2K COLLECTOR RESISTOR RETURNED TO -12V.

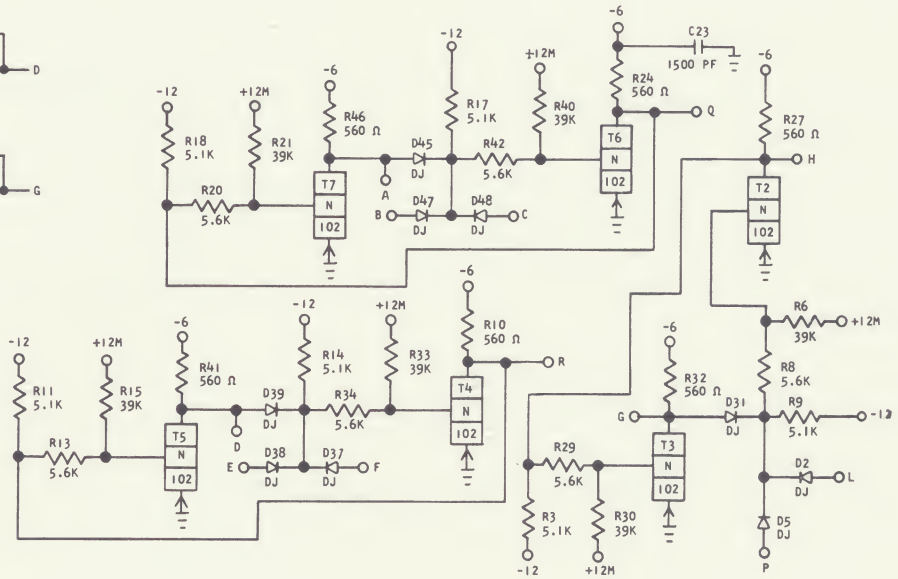
P/N 372191
DHW-

3-D.C. FLIP-FLOPS (SDTDL LATCH)

Ref. Eng. Spec. 892380

TYPICAL APPLICATION*





* CONFIGURATION Ø7 IS NOT A PART OF THE CARD AND IT MUST BE AN UNLOADED LOGIC BLOCK.

OTHER DESIGNATIONS

CONF. 1, 3, 5, 7	+O, -AO, +OA
CONF. 2, 4, 6	I, IO, IA

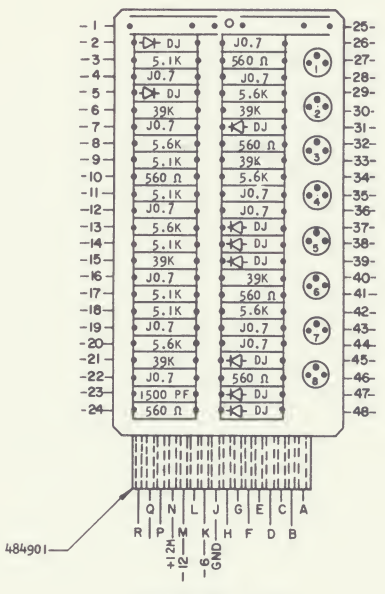
SEQUENCE OF OPERATION (TYPICAL APPLICATION)

1. DOWN LEVEL ON PINS 1 AND 2 CAUSES TRANSISTOR IN SET BLOCK TO TURN ON, OUTPUT (TIED TO PIN Q OF LATCH) TO BE UP.
2. AN UP LEVEL AT INVERTER INPUT RESULTS IN DOWN LEVEL AT THE OUTPUT.
3. ALL INPUTS TO -A BLOCK OF LATCH DOWN, TRANSISTOR TURNS ON. LATCH IS NOW SET.
4. ALL LEVELS ON LATCH REMAIN STABLE, EVEN WHEN SET INPUT LEVELS CHANGE.
5. AN UP LEVEL ON PINS B OR C CAUSES TRANSISTOR IN -A BLOCK OF LATCH TO TURN OFF, OUTPUT (PIN Q) GOES DOWN. LATCH IS NOW RESET.

PINS		SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
1	Y	SET INPUT		UP	-.65V	-.1V
				DOWN	-5.81V	-8.8V
2	Y	SET INPUT	SET … SET	UP	-.65V	-.1V
				DOWN	-5.81V	-8.8V
A	Y	OUTPUT	⊢ STORAGE ⊣	UP	-.65V	-.1V
				DOWN	-5.81V	-8.8V
B	Y	RESET INPUT	RESET	UP	-.65V	-.1V
				DOWN	-5.81V	-8.8V
C	Y	RESET INPUT	RESET	UP	-.65V	-.1V
				DOWN	-5.81V	-8.8V
Q	Y	OUTPUT	⊢ STORAGE ⊣	UP	-.65V	-.1V
				DOWN	-5.81V	-8.8V

DELAY - MSEC

		MIN	MAX
PINS A, B OR C TO PIN Q	TURN ON	75	100
	TURN OFF	40	200
PIN Q TO PIN A	TURN ON	75	100
	TURN OFF	40	200

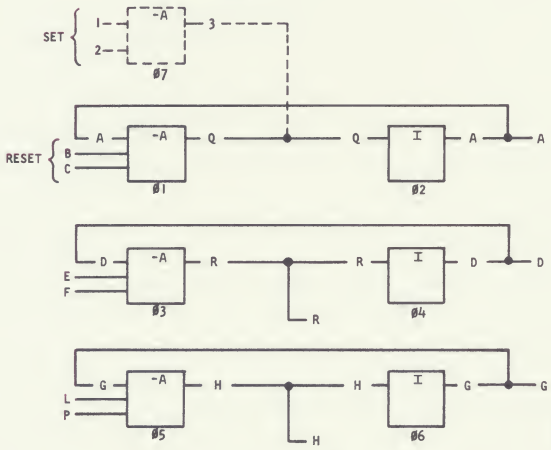


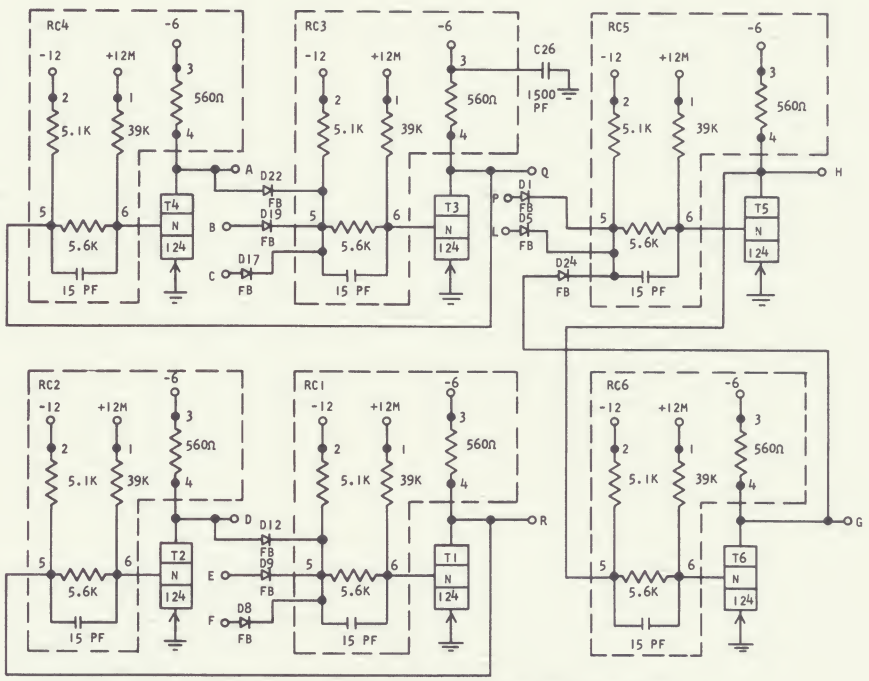
COMPONENT SIDE

P/N 372603
ZGU-
Ref. Eng. Spec. 870585

3-D.C. FLIP-FLOPS, h.s. (SDTDL LATCH)

TYPICAL APPLICATION





* CONFIGURATION Ø7 IS NOT A PART OF THE CARD AND IT MUST BE AND UNLOADED H.S. LOGIC BLOCK.

OTHER DESIGNATIONS

CONF. 1, 3, 5, 7	+O, -AO, +OA
CONF. 2, 4, 6	I, IO, IA

SEQUENCE OF OPERATION (TYPICAL APPLICATION)

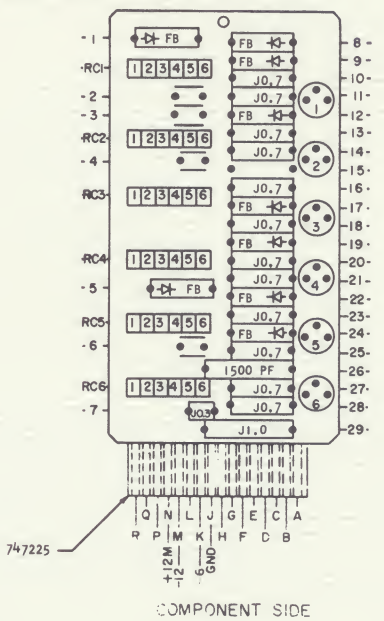
1. DOWN LEVEL ON PINS 1 AND 2 CAUSES TRANSISTOR IN SET BLOCK TO TURN ON, OUTPUT (TIED TO PIN Q OF LATCH) TO BE UP.
2. AN UP LEVEL AT INVERTER INPUT RESULTS IN DOWN LEVEL AT THE OUTPUT.
3. ALL INPUTS TO -A BLOCK OF LATCH DOWN, TRANSISTOR TURNS ON. LATCH IS NOW SET.
4. ALL LEVELS ON LATCH REMAIN STABLE, EVEN WHEN SET INPUT LEVELS CHANGE.
5. AN UP LEVEL ON PINS B OR C CAUSES TRANSISTOR IN -A BLOCK OF LATCH TO TURN OFF, OUTPUT (PIN Q) GOES DOWN. LATCH IS NOW RESET.

PINS		SIGNAL NAME	WAVESHAPE		LEVELS MIN	LEVELS MAX
1	Y	SET INPUT		UP	-.65V	-.1V
				DOWN	-5.81V	-12.48V*
2	Y	SET INPUT	SET SET	UP	-.65V	-.1V
				DOWN	-5.81V	-12.48V*
A	Y	OUTPUT	STORAGE	UP	-.35V	-.1V
				DOWN	-5.81V	-12.48V*
B	Y	RESET INPUT	RESET	UP	-.65V	-.1V
				DOWN	-5.81V	-12.48V*
C	Y	RESET INPUT	RESET	UP	-.65V	-.1V
				DOWN	-5.81V	-12.48V*
Q	Y	OUTPUT	STORAGE	UP	-.35V	-.1V
				DOWN	-5.81V	-12.48V*

* FUNCTION OF LOAD

DELAY - NSEC

		MIN	MAX
PINS A, B OR C TO PIN Q	TURN ON	18	100
	TURN OFF	15	150
PIN Q TO PIN A	TURN ON	18	100
	TURN OFF	15	150

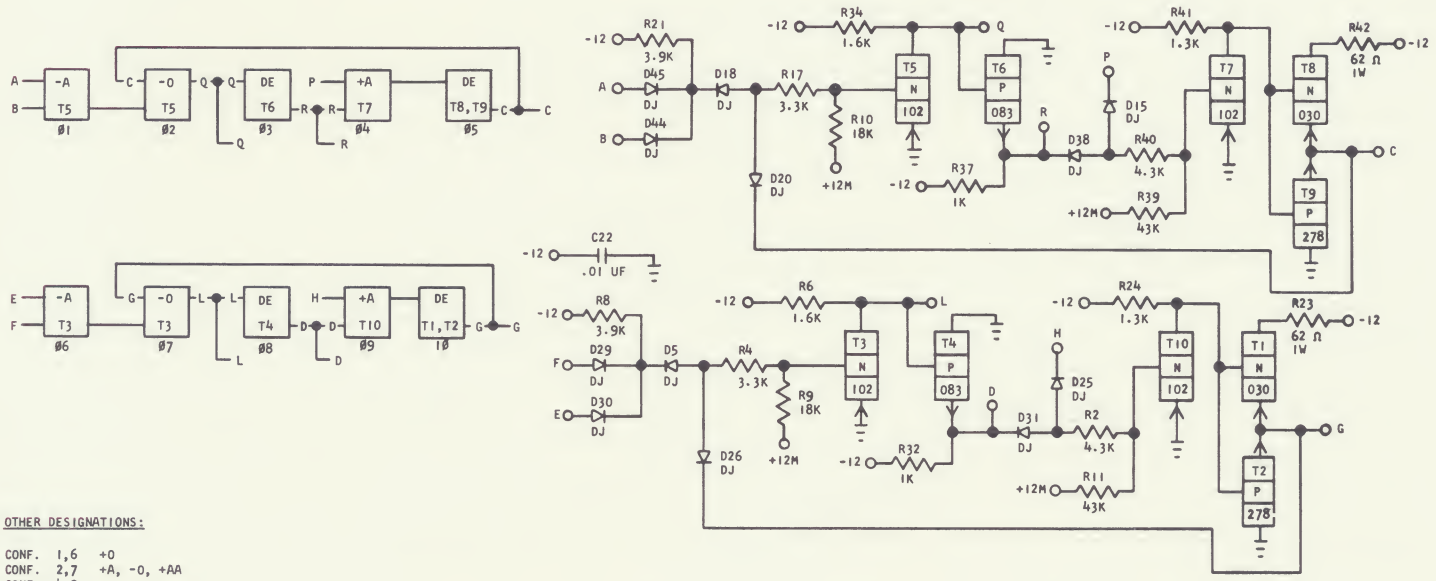


COMPONENT SIDE

2-Two Input NAND FLIP-FLOPS with Complementary Emitter Follower Output

P/N 372237
AXX-
Ref. Eng. Specs. 870196
870201
870244
892226

SDTDL POWER LATCH A



OTHER DESIGNATIONS:

CONF. 1,6 +O
CONF. 2,7 +A, -O, +AA
CONF. 4,9 -O

SEQUENCE OF OPERATION

1. THE FIRST SET OF DIODES TO T5 AND T3 PERFORM A NEGATIVE AND FUNCTION AND THE SECOND SET A NEGATIVE OR.
2. THE LATCH OPERATION IS PERFORMED BY COUPLING THE OUTPUT OF T8 AND T9 BACK TO THE NEGATIVE OR OF T5 AND THE OUTPUT OF T1 AND T2 BACK TO THE NEGATIVE OR OF T3.
3. WHEN THE OUTPUT IS DOWN THE CIRCUIT LATCHES BACK AND HOLDS T5 OR T3 ON UNTIL THE CIRCUIT IS RESET.

NOTE:

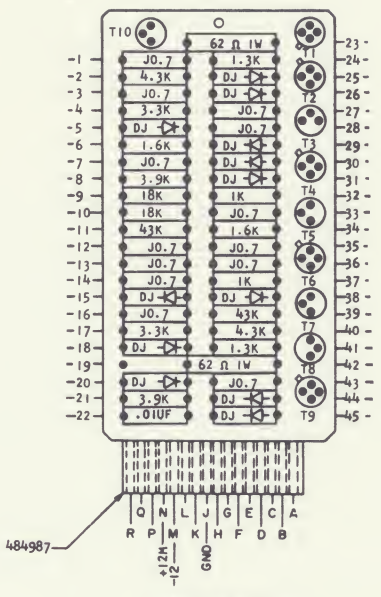
THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF THE BLOCK DIAGRAM REFER TO TRANSISTORS ON THE CARD.

PINS	SIGNAL NAME		WAVESHAPE	LEVELS	MIN	MAX
A,E	Y	INPUT	SET	UP	-.65V	-.1V
				DOWN	-5.28V	-12.48V
B,F	Y	INPUT		UP	-.65V	-.1V
				DOWN	-5.28V	-12.48V
L,Q	Y	OUTPUT	STORAGE	UP	-.65V	-.1V
				DOWN	-5.81V	-12.48V
R,D	Y	OUTPUT	STORAGE	UP	-1.10V	-.22V
				DOWN	-5.83V	-7.30V
P,H	Y	INPUT	RESET	UP	-.65V	-.05V
				DOWN	-5.5V	-8.8V
C,G	Y	OUTPUT	STORAGE	UP	-1.25V	-.05V
				DOWN	-6.71V	-6.71V*

* FUNCTION OF I_C

DELAY - NSEC

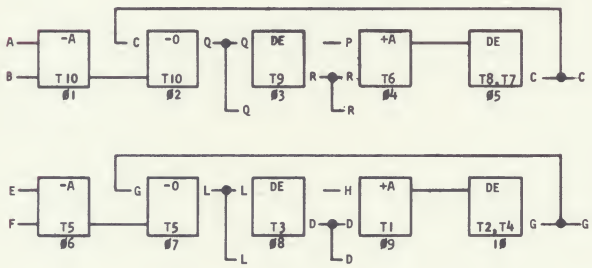
		MIN	MAX
PINS A, B, E OR F TO PINS Q OR L	TURN ON	70	240
	TURN OFF	110	515
PINS Q OR L TO PINS R OR D	TURN ON	6	20
	TURN OFF	6	28
PINS P, R, H OR D TO PINS C OR G	TURN ON	145	170
	TURN OFF	90	250



COMPONENT SIDE

2-Two Input NAND FLIP-FLOPS with Complementary Emitter Follower Outputs, h.s.

P/N 372526
DKW-
Ref. Eng. Specs. 870196
870244
870529
892226



OTHER DESIGNATIONS

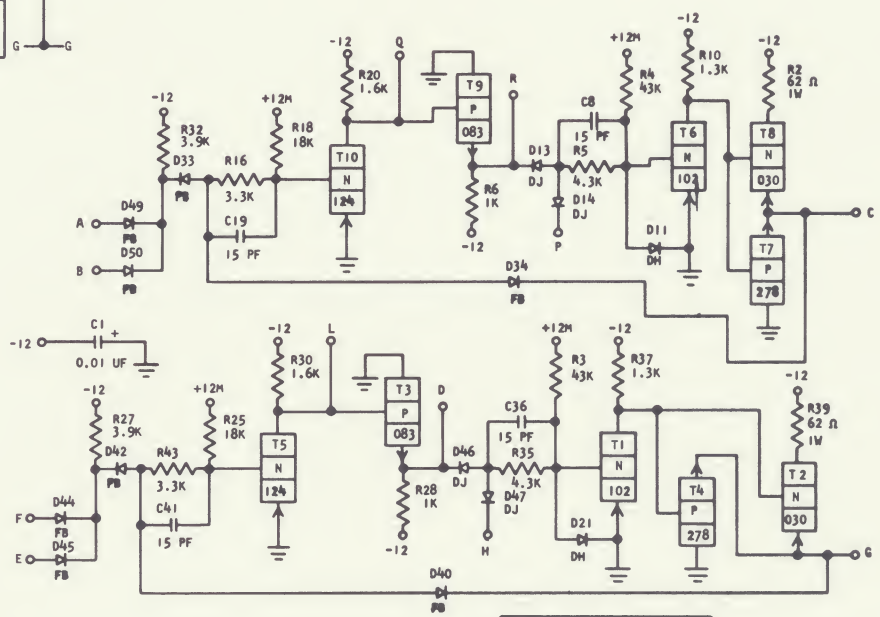
CONF. 1, 6 +0
CONF. 2, 7 +A, -0, +AA
CONF. 4, 9 -0

SEQUENCE OF OPERATION

1. THE FIRST SET OF DIODES TO T10 AND T5 PERFORM A NEGATIVE AND FUNCTION AND THE SECOND SET A NEGATIVE OR.
2. THE LATCH OPERATION IS PERFORMED BY COUPLING THE OUTPUT OF T7 AND T8 BACK TO THE NEGATIVE OR OF T10 AND THE OUTPUT OF T2 AND T4 BACK TO THE NEGATIVE OR OF T5.
3. WHEN THE OUTPUT IS DOWN THE CIRCUIT LATCHES BACK AND HOLDS T5 OR T3 ON UNTIL THE CIRCUIT IS RESET.

NOTE

THE ONE AND TWO DIGIT NUMBERS SHOWN IN THE INDIVIDUAL BLOCKS OF THE BLOCK DIAGRAM REFER TO TRANSISTORS ON THE CARD.

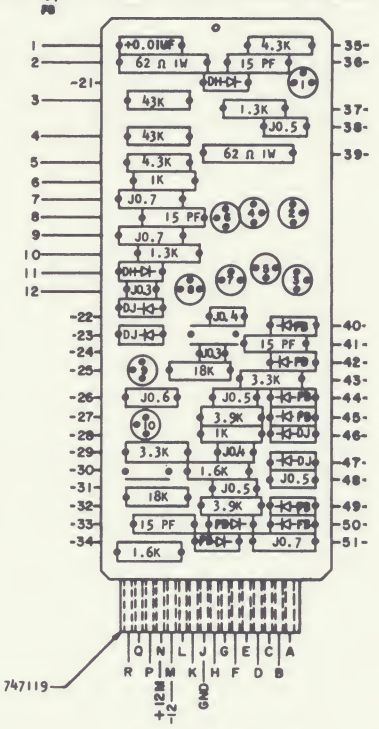


PINS		SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
A,E	Y	INPUT		UP	-.65V	-.1V
				DOWN	-5.28V	-12.48V
B,F	Y	INPUT	SET	UP	-.65V	-.1V
				DOWN	-5.28V	-12.48V
L,Q	Y	OUTPUT	STORAGE	UP	-0.35V	-.1V
				DOWN	-5.81V	-12.48V
R,D	Y	OUTPUT	STORAGE	UP	-1.10V	-.22V
				DOWN	-5.83V	-7.30V
P,H	Y	INPUT	RESET	UP	-.65V	-.05V
				DOWN	-5.5V	-8.8V
C,G	Y	OUTPUT	STORAGE	UP	-1.25V	-.05V
				DOWN	-6.71V	-6.71V*

* FUNCTION OF I_C

DELAY - NSEC

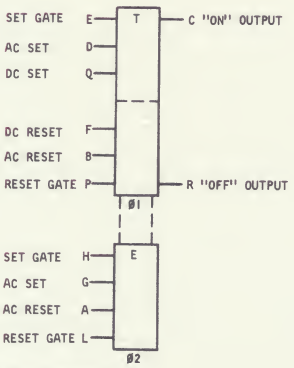
		MIN	MAX
PINS A, B, E OR F TO PINS Q OR L	TURN ON	15	280
	TURN OFF	24	300
PINS Q OR L TO PINS R OR D	TURN ON	6	20
	TURN OFF	6	28
PINS P, R, H OR D TO PINS C OR G	TURN ON	51	76
	TURN OFF	62	132



COMPONENT SIDE

1-FLIP-FLOP, Dual Gated AC Set and Reset, D.C. Set and Reset

P/N 372239
AXZ-
Ref. Eng. Spec. 870239



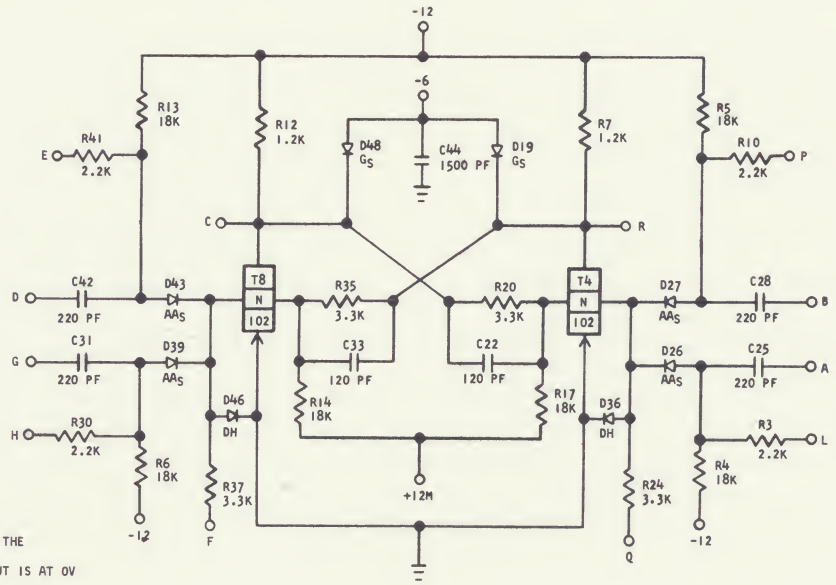
OTHER DESIGNATIONS
T8

SEQUENCE OF OPERATION

1. WHEN THE TRIGGER IS SET, THE "ON" OUTPUT IS AT -6V AND THE "OFF" OUTPUT IS 0V.
2. WHEN THE TRIGGER IS IN A RESET CONDITION THE "ON" OUTPUT IS AT 0V AND THE "OFF" OUTPUT IS AT -6V.
3. TRIGGER IS SET BY
   A) A NEGATIVE VOLTAGE LEVEL APPLIED TO THE DC SET INPUT OR
   B) AN UP LEVEL AT THE SET GATE INPUT IN CONJUNCTION WITH A POSITIVE SHIFT AT THE AC SET INPUT.
4. TRIGGER IS RESET BY
   A) A NEGATIVE VOLTAGE LEVEL AT THE DC RESET INPUT OR
   B) AN UP LEVEL AT THE RESET GATE INPUT IN CONJUNCTION WITH A POSITIVE SHIFT AT THE AC RESET INPUT.

NOTES:

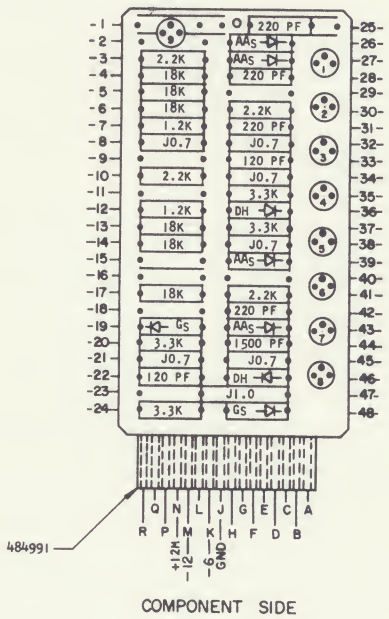
1. THE GATES MUST BE AT THE UP LEVEL 150 NS BEFORE THE AC SET ARRIVES.
2. THE AC SET SHOULD BE AT LEAST 70 NS WIDE AND ITS RISE TIME 70 NS OR LESS.



PINS		SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
E H	Y	SET GATE		UP	-.65V	-.05V
				DOWN	-5.81V	-7.64V
D G	Y	AC SET		UP	-.65V	-.05V
				DOWN	-5.81V	-7.64V
B A	Y	AC RESET		UP	-.65V	-.05V
				DOWN	-5.81V	-7.64V
P L	Y	RESET GATE		UP	-.65V	-.05V
				DOWN	-5.81V	-7.64V
Q	Y	DC SET		UP	-.65V	-.05V
				DOWN	-6.26V	-7.64V
F	Y	DC RESET		UP	-.65V	-.05V
				DOWN	-6.26V	-7.64V
C	Y	"ON" OUTPUT		UP	-.65V	-.05V
				DOWN	-6.26V	-7.64V
R	Y	"OFF" OUTPUT		UP	-.65V	-.05V
				DOWN	-6.26V	-7.64V

DELAY - NSEC

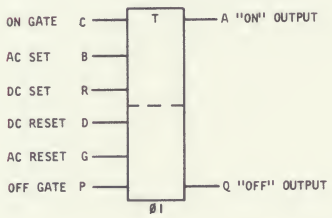
	TON MAX	TON MIN	TRISE MAX	TRISE MIN	TOFF MAX	TOFF MIN	TFALL MAX	TFALL MIN
BINARY OPERATION:	340	40	50	25	825	175	635	155
GATED:	350	35	50	20	685	125	475	110



COMPONENT SIDE

1-FLIP-FLOP, Gated AC Set and Reset, D.C. Set and Reset, h.s.

P/N 372575
HFT-
Ref. Eng. Spec. 870575



OTHER DESIGNATIONS

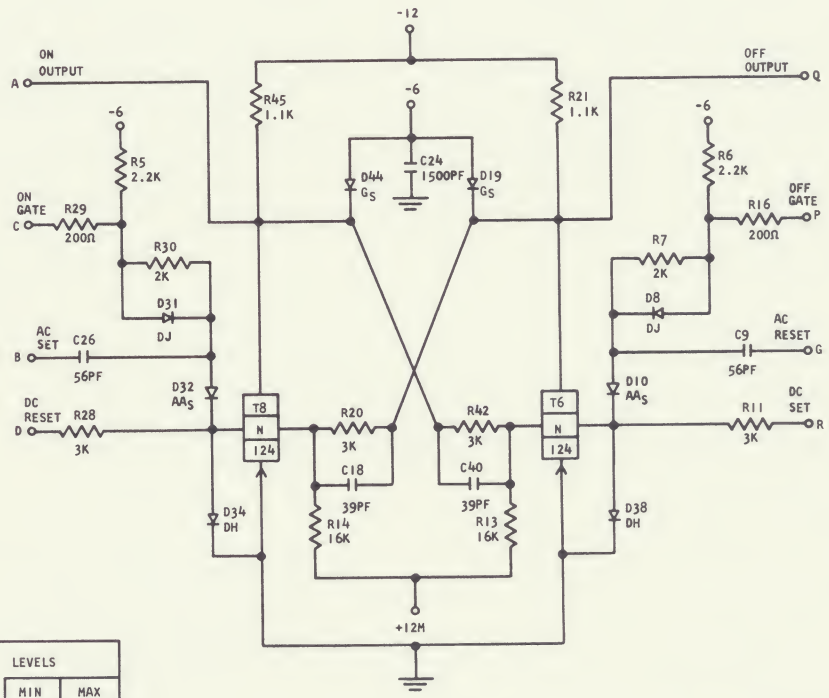
TB

SEQUENCE OF OPERATION

1. WHEN THE TRIGGER IS SET, THE "ON" OUTPUT IS AT -6V AND THE "OFF" OUTPUT IS 0V.
2. WHEN THE TRIGGER IS IN A RESET CONDITION THE "ON" OUTPUT IS AT 0V AND THE "OFF" OUTPUT IS AT -6V.
3. TRIGGER IS SET BY
   (A) A NEGATIVE VOLTAGE LEVEL APPLIED TO THE DC SET INPUT OR
   (B) AN UP LEVEL AT THE SET GATE INPUT IN CONJUNCTION WITH A POSITIVE SHIFT AT THE AC SET INPUT.
4. TRIGGER IS RESET BY
   (A) A NEGATIVE VOLTAGE LEVEL AT THE DC RESET INPUT OR
   (B) AN UP LEVEL AT THE RESET GATE INPUT IN CONJUNCTION WITH A POSITIVE SHIFT AT THE AC RESET INPUT.

NOTES:

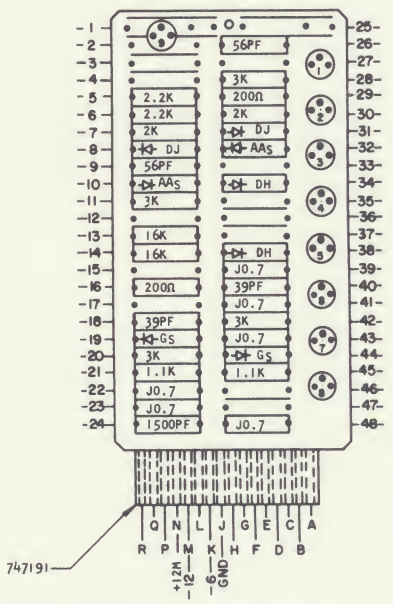
1. THE GATES MUST BE AT THE UP LEVEL 150 NS BEFORE THE AC SET ARRIVES.
2. THE AC SET SHOULD BE AT LEAST 70 NS WIDE AND ITS RISE TIME 70 NS OR LESS.



PINS		SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
C	Y	ON GATE		UP	-0.65V	-0.05V
				DOWN	-5.81V	-7.64V
B	Y	AC SET		UP	-0.65V	-0.05V
				DOWN	-5.81V	-7.64V
G	Y	AC RESET		UP	-0.65V	-0.05V
				DOWN	-5.81V	-7.64V
P	Y	OFF GATE		UP	-0.65V	-0.05V
				DOWN	-5.81V	-7.64V
R	Y	DC SET		UP	-0.65V	-0.05V
				DOWN	-5.81V	-7.64V
D	Y	DC RESET		UP	-0.65V	-0.05V
				DOWN	-5.81V	-7.64V
A	Y	"ON" OUTPUT		UP	-0.65V	-0.05V
				DOWN	-6.26V	-7.64V
Q	Y	"OFF" OUTPUT		UP	-0.65V	-0.05V
				DOWN	-6.26V	-7.64V

DELAY - NSEC

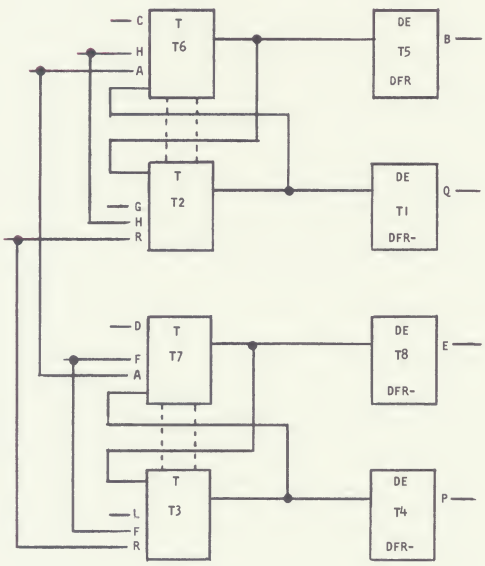
	T_{ON}		T_{RISE}		T_{OFF}		T_{FALL}	
	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN
BINARY OPERATION:	133	36	63	16	240	115	200	95
GATED:	135	40	60	16	255	82	210	61



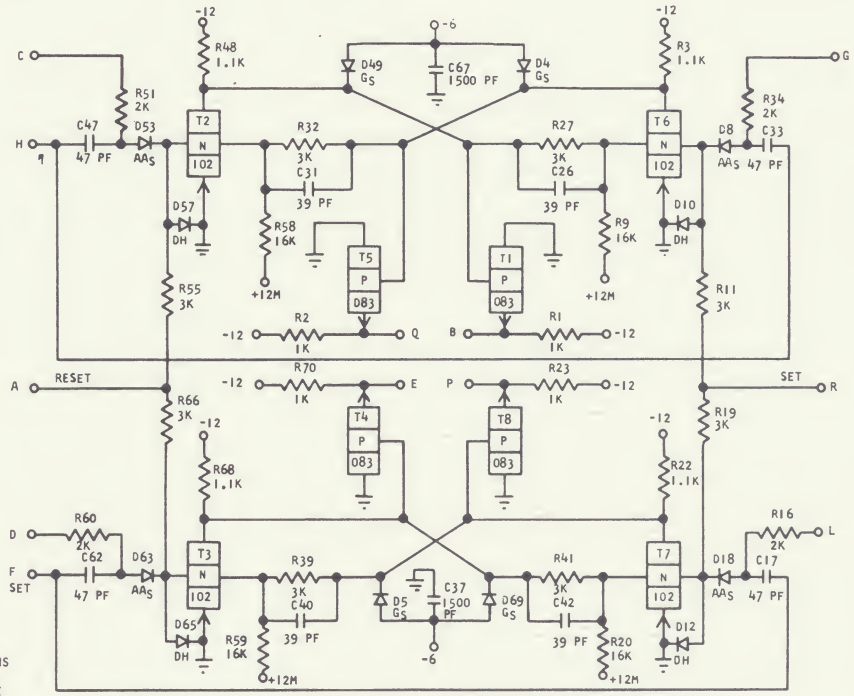
COMPONENT SIDE

2-FLIP-FLOPS, Gated AC Set, Common D.C. Set and Reset, Emitter Follower Outputs

P/N 370350
DHF-
Ref. Eng. Specs. 892222
892226



TRIGGER AND DRIVER



SEQUENCE OF OPERATION

THE RESET INPUT RESPONDS TO A NEGATIVE VOLTAGE LEVEL. RESETTING TURNS T6,T7,T5 AND T8 ON AND THE OTHER TRANSISTORS WILL BE IN THE OPPOSITE STATE. THE GATES ARE CONDITIONED BY A POSITIVE VOLTAGE LEVEL AND THE AC SET IS RESPONSIVE TO A POSITIVE VOLTAGE LEVEL. THUS, TO SET THE TRIGGER MEANS TO TURN OFF THE TRANSISTOR WHOSE GATE AND SET ARE BOTH POSITIVE. THE DC SET RESPONDS TO A NEGATIVE VOLTAGE LEVEL. THUS, WHEN THE TRIGGER IS DC SET, T2,T3,TI AND T4 WILL BE ON.

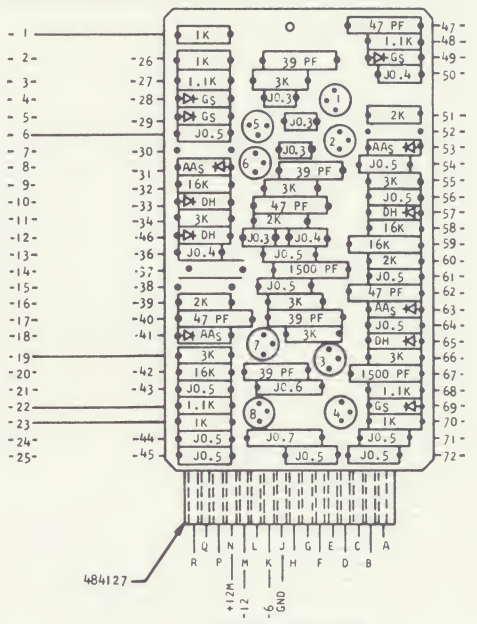
DELAY - NSEC	T_{ON} MAX	T_{ON} MIN	T_{RISE} MAX	T_{RISE} MIN	T_{OFF} MAX	T_{OFF} MIN	T_{FALL} MAX	T_{FALL} MIN
BINARY OPERATION:	123	36	63	16	240	115	200	95
GATED:	135	40	48	16	205	82	160	61

NOTE: T_{ON} IS DEFINED AS THE DELAY FROM THE TIME AN AC INPUT SIGNAL ARRIVES UNTIL THE "OFF" TRANSISTOR HAS TURNED ON COMPLETELY. THIS IS MEASURED FROM THE TIME THE AC INPUT HAS SHIFTED 10%.

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
C,D	Y	GATE		UP	-.65	-.1
				DOWN	-5.81	-7.64
H,F	Y	AC SET		UP	-.65	-.1
				DOWN	-5.81	-7.64
R	Y	DC SET		UP	-.65	-.1
				DOWN	-5.81	-7.64
A	Y	RESET		UP	-.65	-.1
				DOWN	-5.81	-7.64
Q,P	Y	OUTPUT		UP	-1.1	-7.3
				DOWN	-5.83	-7.3
B,E	Y	OUTPUT		UP	-1.1	-.22
				DOWN	-5.83	-7.3
G,L	Y	GATE		UP	-.65	-.1
				DOWN	-5.81	-7.64

IN THE POSITIVE DIRECTION UNTIL THE "OFF" TRANSISTOR HAS SHIFTED 90% POSITIVE.

T_{OFF} IS MEASURED FROM THE TIME AN AC INPUT HAS SHIFTED 10% POSITIVE UNTIL THE OUTPUT OF THE "ON" TRANSISTOR HAS SHIFTED 90% NEGATIVE.

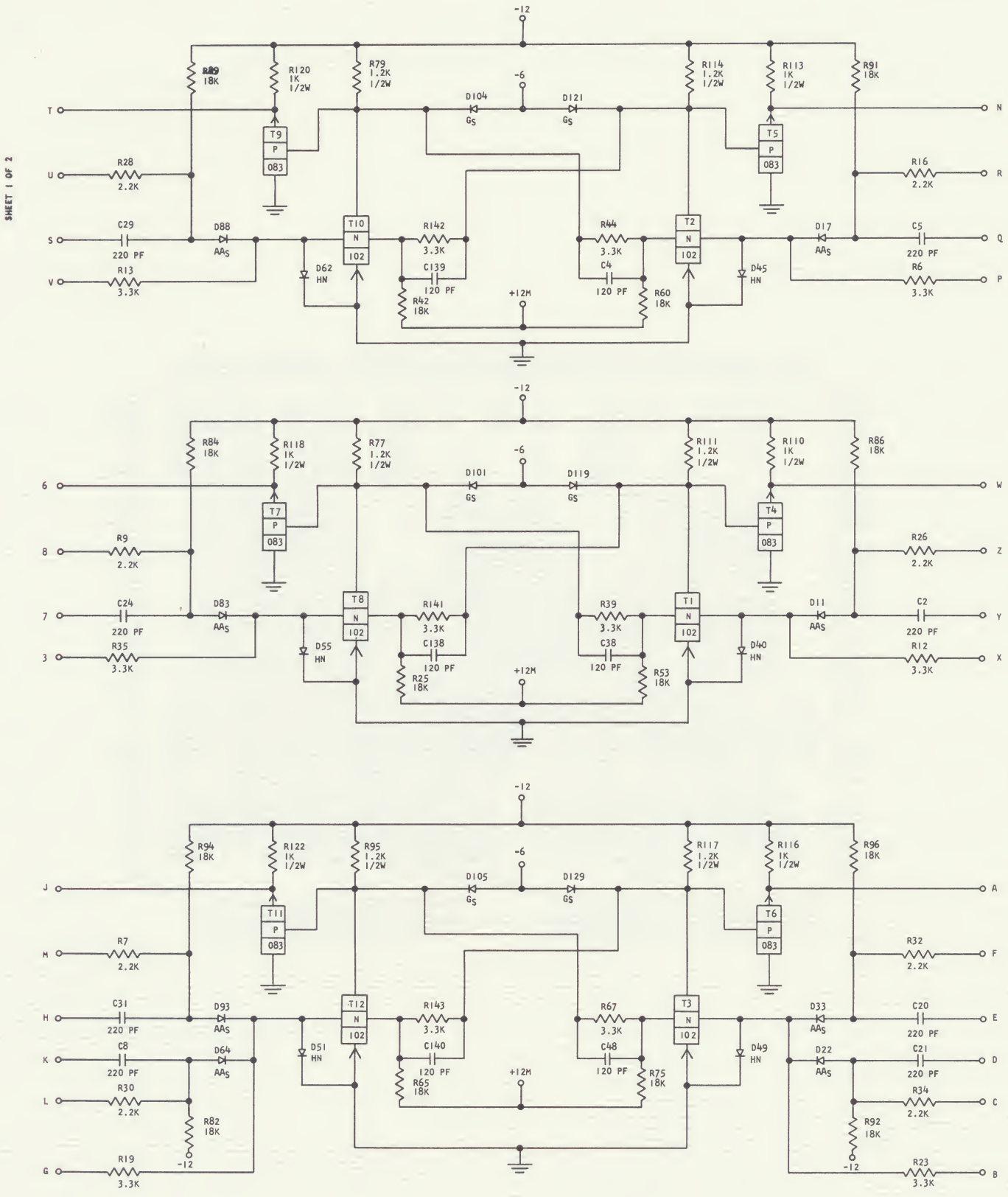


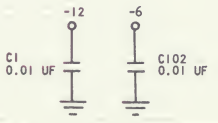
COMPONENT SIDE

3-FLIP-FLOPS, Gated AC Set and Reset, D.C. Set and Reset, Emitter Follower Outputs

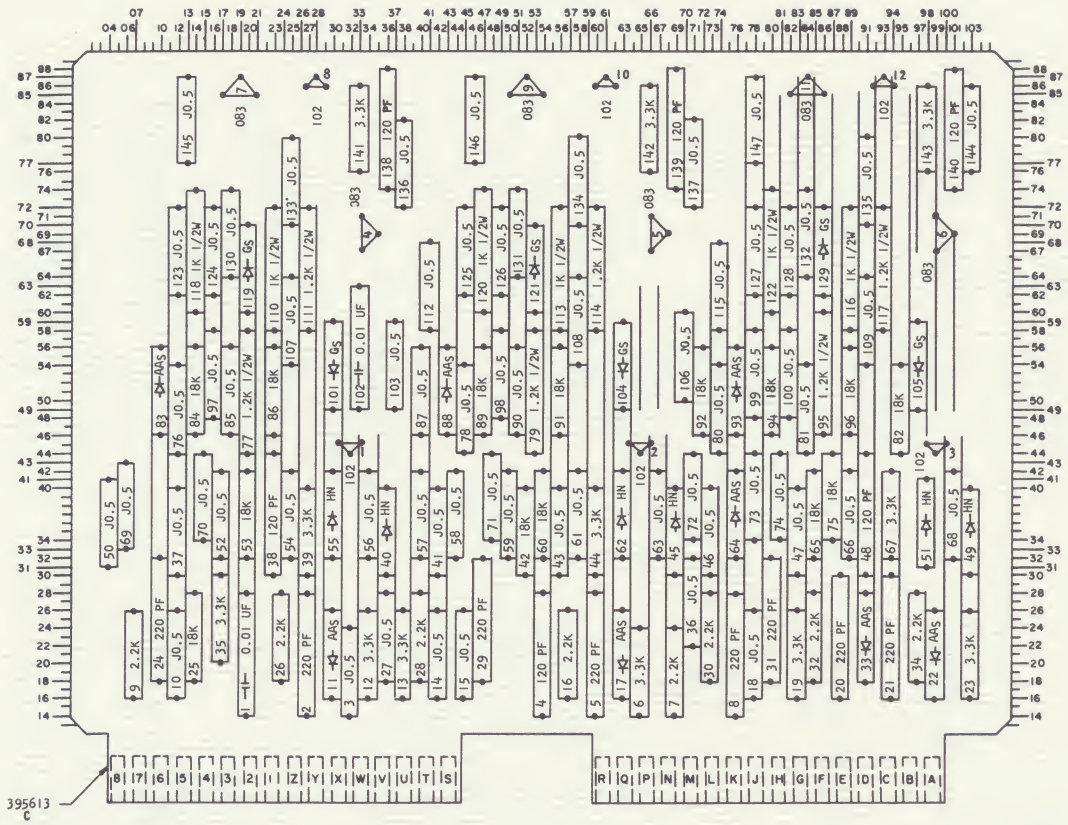
P/N 373316
ADC-
Ref. Eng. Specs. 870239
892226

SHEET 1 OF 2



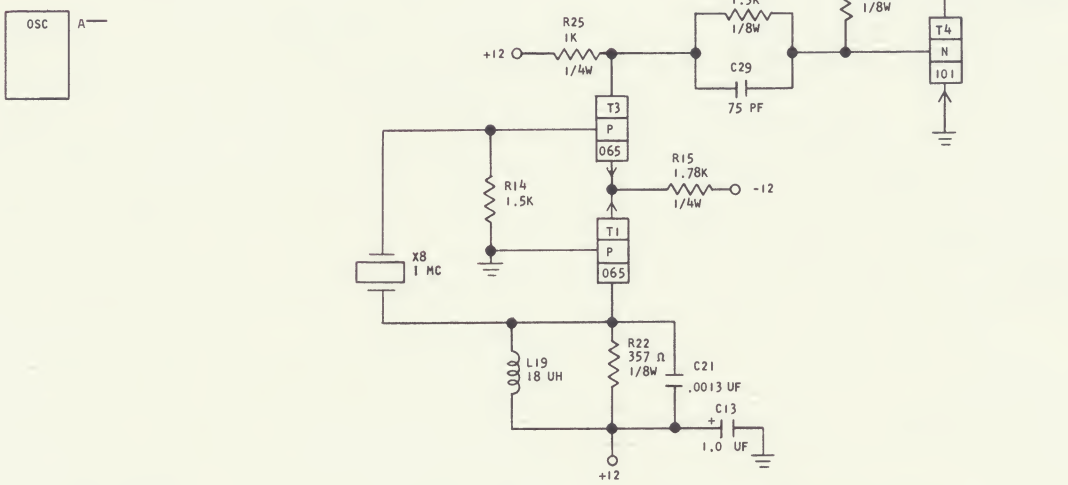


VOLTAGE	PIN
GND	1
-6	2
-12	4
+12M	5


395613
C

P/N 370551
TDK-
Ref. Eng. Spec. 892551

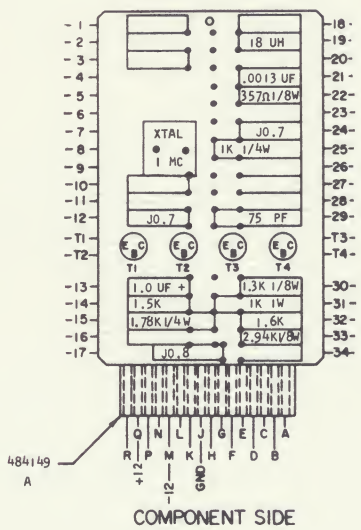
1 MC. Oscillator, Crystal Controlled



SEQUENCE OF OPERATION

1. WHEN POWER IS UP, THE OSCILLATOR TURNS ON.
2. PIN A CAN BE TIED TO TWO DIFFERENT LOADS DEPENDING ON CURRENT REQUIREMENTS.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS		
					MIN	MAX
A	S	OUTPUT	1MC	UP	-.3	0
				DOWN	-5.8	-12.48

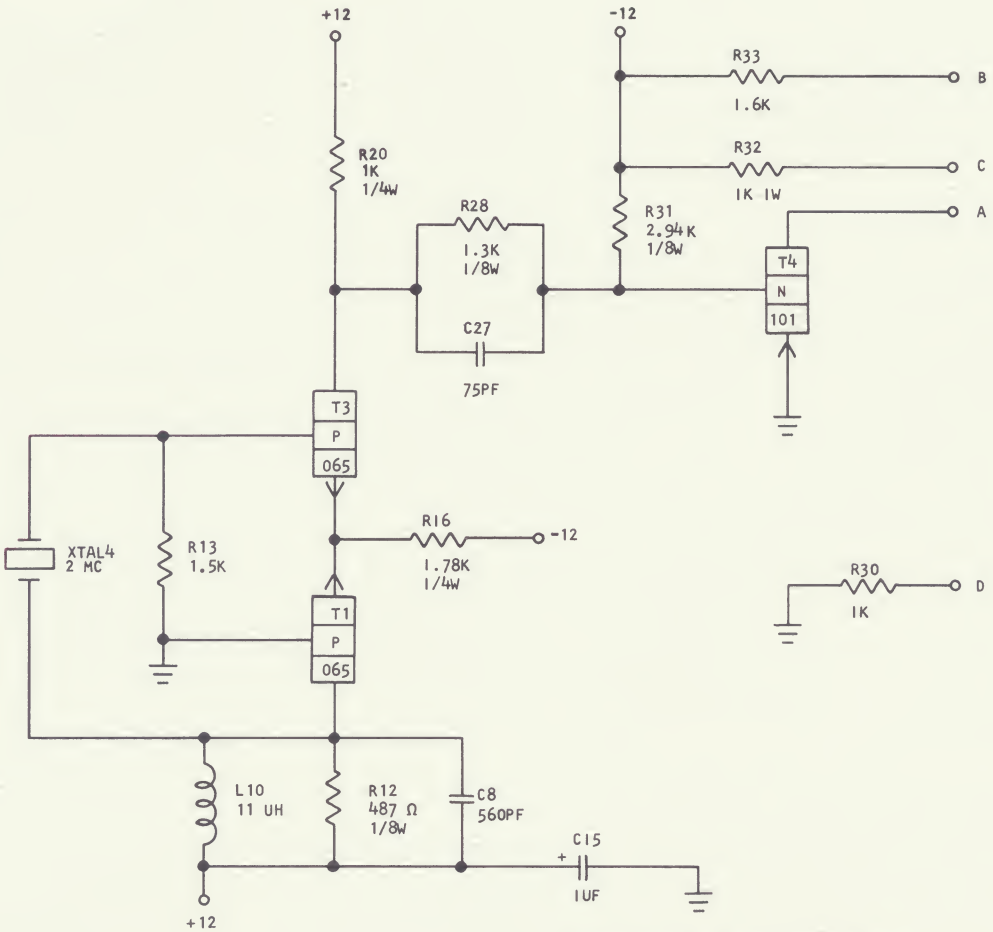


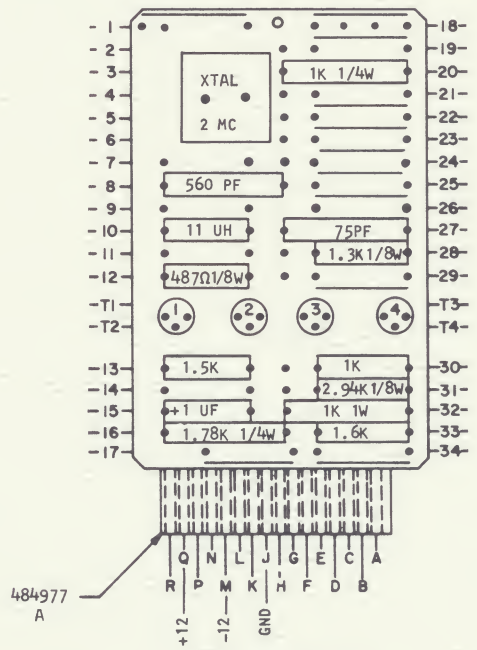
COMPONENT SIDE

P/N 372231
TNC-

2 MC. Oscillator, Crystal Controlled

Ref. Eng. Spec. 870231

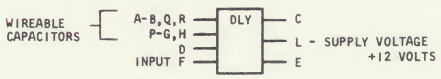


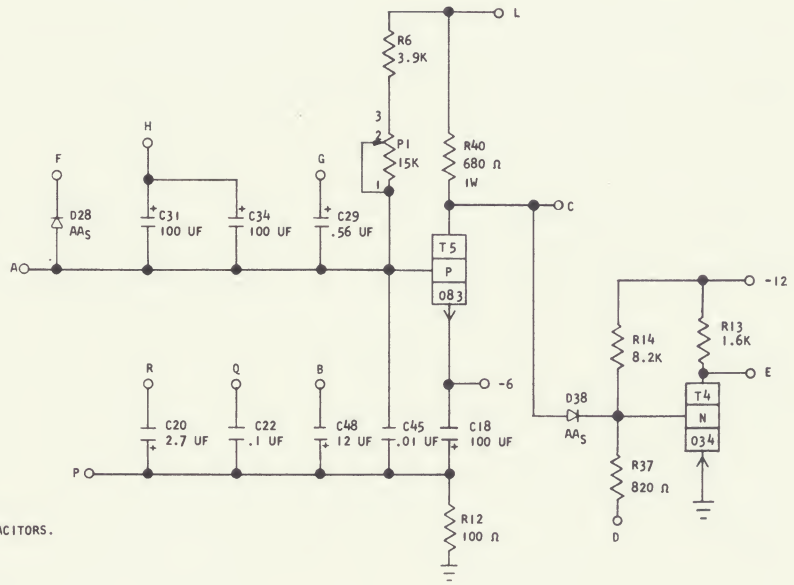


COMPONENT SIDE

P/N 370703
AQQ-
Ref. Eng. Spec. 892703

General Delay, Variable





SEQUENCE OF OPERATION

1. INPUT LEVEL DOWN, OUTPUT C UP, OUTPUT E DOWN.
2. INPUT SWITCHING TO UP LEVEL, OUTPUT C DELAYED THEN SWITCHES TO DOWN LEVEL. OUTPUT E DELAYED THEN SWITCHES TO UP LEVEL.
3. THE DELAY OF THE POSITIVE EDGE IS DETERMINED BY THE WIREABLE CAPACITORS. THE OUTPUT REMAINS AS LONG AS INPUT REMAINS UP.

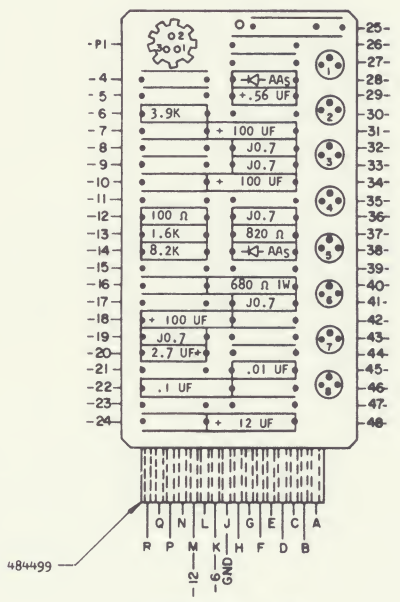
NOTE: PIN D GROUNDED

PINS	SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
F	INPUT		UP	-5.31V	+.24V
			DOWN	-6.95V	-12.48V
E	OUTPUT		UP	-.54V	+.24V
			DOWN	-5.81V	-12.48V
C	OUTPUT		UP	+1.44V	+6.7V
			DOWN	-4.47V	-6.24V

DELAY*

	POT SET AT 0K	POT SET AT 15K
INPUT F	7 USEC	34 USEC
A-Q	72 USEC	370 USEC
P-G	300 USEC	1.75 MSEC
A-R	1.80 MSEC	9 MSEC
A-B	9 MSEC	39 MSEC
P-H	140 MSEC	650 MSEC

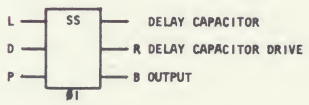
* DELAY IS MEASURED FROM THE TIME D28 REVERSE BIASES TO WHEN OUTPUT C CROSSES GROUND.



COMPONENT SIDE

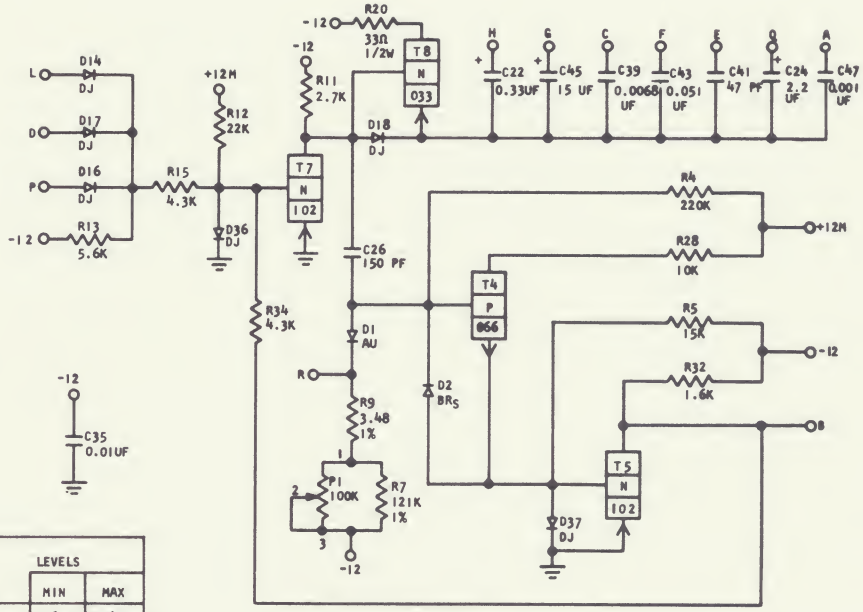
P/N 372275
AZK-
Ref. Eng. Spec. 870275

Single Shot, Variable



SEQUENCE OF OPERATION

1. OPERATION IS INITIATED BY COINCIDENCE OF DOWN LEVELS ON PINS L, D, AND P. T7 TURNS ON AND ITS OUTPUT IS COUPLED THROUGH C26 TO TURN ON T4. T5 TURNS OFF AND THE OUTPUT IS DOWN FOR THE DURATION OF THE DELAY TIME.
2. RESET TO THE OFF CONDITION IS AUTOMATIC AT THE END OF THE DELAY TIME.



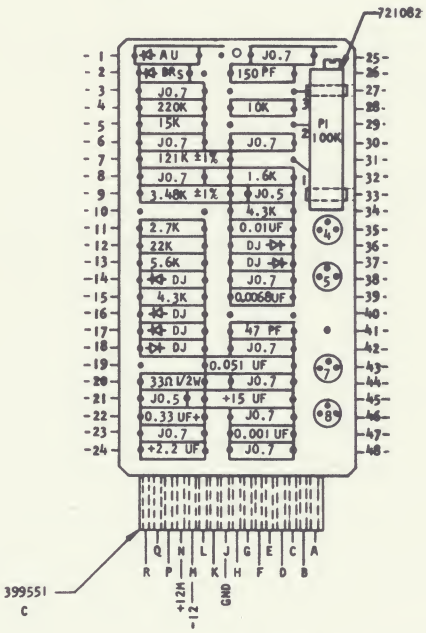
PINS	SIGNAL NAME	WAVESHAPE	LEVELS	MIN	MAX
L	Y INPUT		UP	-.65V	+.24V
			DOWN	-5.81V	-12.48V
D	Y INPUT		UP	-.65V	+.24V
			DOWN	-5.81V	-12.48V
P	Y INPUT		UP	-.65V	+.24V
			DOWN	-5.81V	-12.48V
B	Y OUTPUT	*DELAY TIME	UP	-.65V	-.05V
			DOWN	-5.81V	-9.51V

* THE DELAY TIME IS DETERMINED BY THE CAPACITOR WIRED TO PIN R AND THE SETTING OF THE DELAY POTENTIOMETER.

DELAY

	MIN	MAX
T_{ON} (NSEC)	30	380
T_{OFF} (NSEC)	390	340

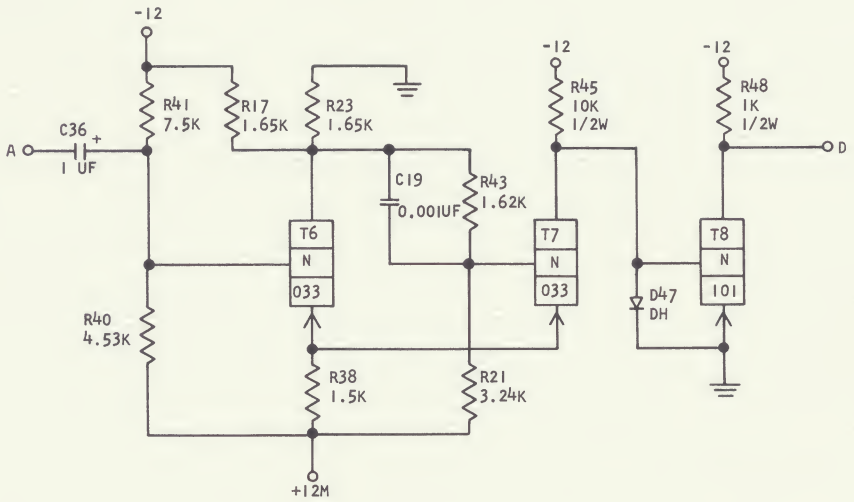
WIRE PIN R TO	FOR PULSE WIDTHS FROM - TO
E	.39 US - 3.0 US
A	2.9 US - 21 US
AC	21 US - 167 US
F	143 US - 1.1 MS
ACH	.94 MS - 7.29 MS
HQ	7.4 MS - 63 MS
GQ	51 MS - 340 MS

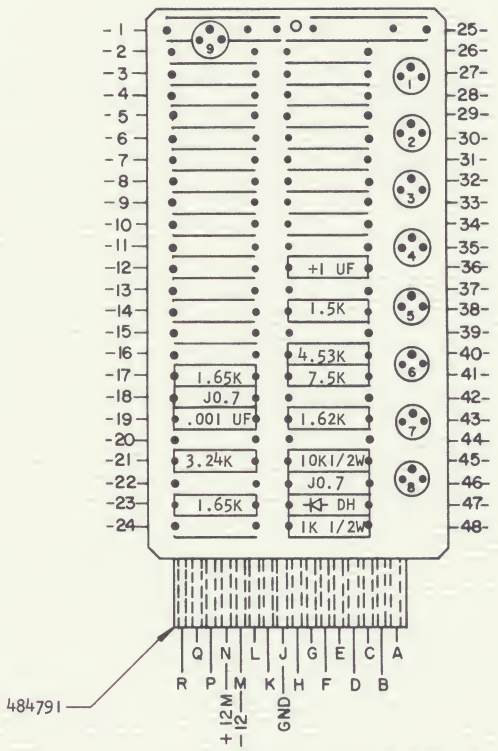


COMPONENT SIDE

Schmitt Trigger

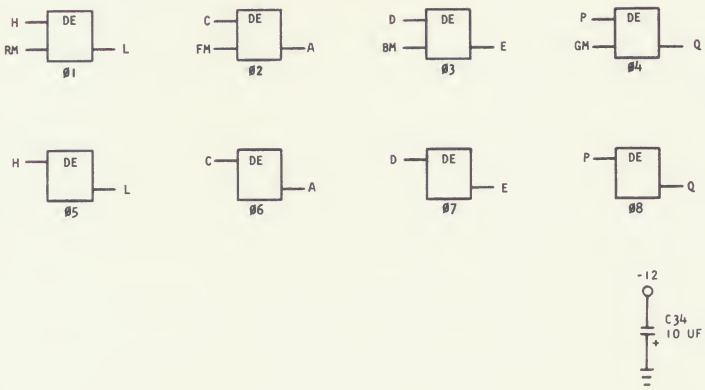
P/N 370885
TFW-
Ref. Eng. Spec. 892885

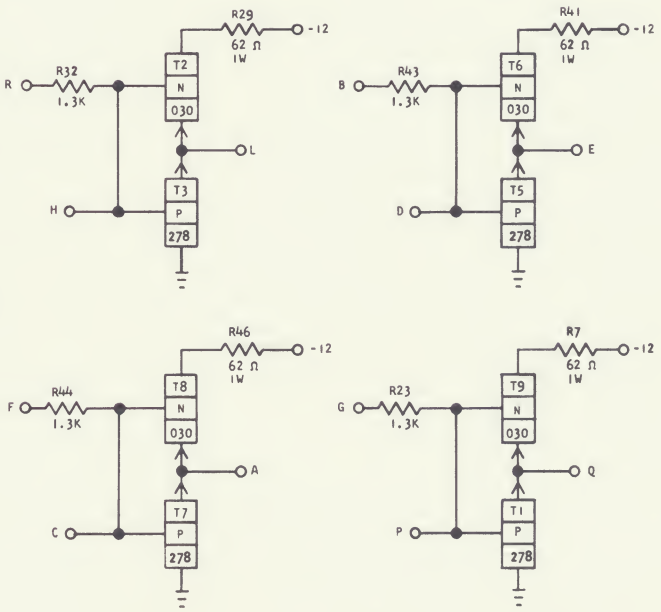




P/N 372244
AXV-
Ref. Eng. Spec. 870244

4-Complementary Emitter Followers, high powered





SEQUENCE OF OPERATION

1. INPUT UP: TRANSISTOR (T3) ON, OUTPUT UP.

2. INPUT DOWN: TRANSISTOR (T2) ON, OUTPUT DOWN.

NOTES: 1. CONF. ø1-ø4 MAY ONLY BE DRIVEN BY UNLOADED BLOCKS DUE TO THE 1.3K RESISTOR TIED TO -12V.

2. CONF. ø5-ø8 ARE USED WHEN DRIVEN BY A CLAMPED LOGIC BLOCK, IP, OR TRIGGER.

PINS	SIGNAL NAME		WAVESHAPE		LEVELS MIN	LEVELS MAX
H	Y	INPUT		UP	-.65V	-.05V
				DOWN	-6V	*
L	Y	OUTPUT		UP	+1.25V	-.05V
				DOWN	-6.71V	-6.71V[1]
H	Y	INPUT		UP	+.65V	-.05V
				DOWN	-6V	*
L	Y	OUTPUT		UP	+1.25V	-.05V
				DOWN	-5.51V	-6.69V[2]

* FUNCTION OF CURRENT SWITCHED.

1. DRIVEN BY LOGIC BLOCK.

2. DRIVEN BY IP, TRIGGER OR CLAMPED LOGIC BLOCK.

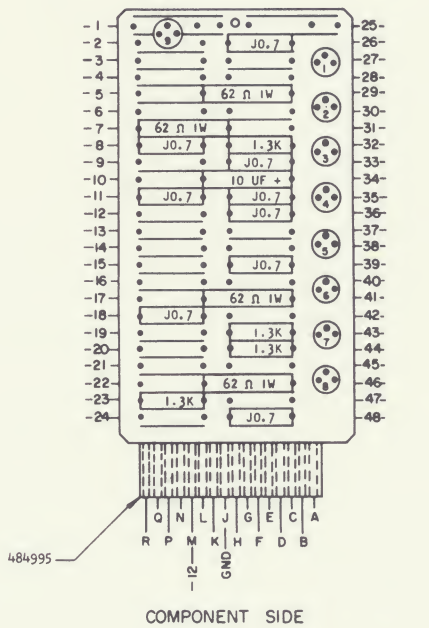
DELAY-MAXIMUM

LOW SPEED DRIVERS:

	TURN ON (NSEC)	TURN OFF (NSEC)
LOGIC BLOCK	70	50
CLAMPED LOGIC BLOCK	24	28
I.P.	36	20

HIGH SPEED DRIVERS:

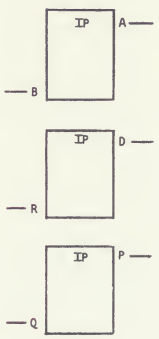
	TURN ON (NSEC)	TURN OFF (NSEC)
LOGIC BLOCK	46	52
CLAMPED LOGIC BLOCK	39	32
I.P.	56	21



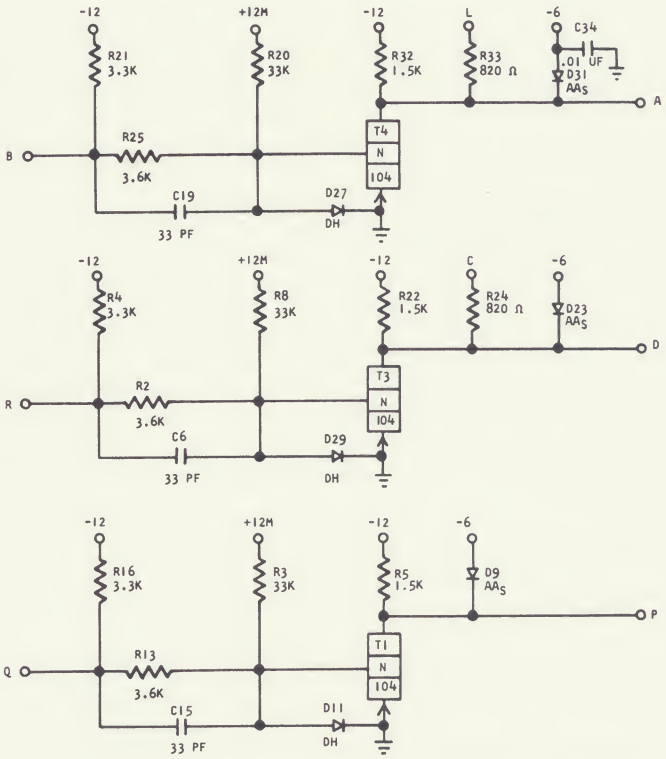
COMPONENT SIDE

P/N 370225
DFQ-
Ref. Eng. Spec. 892225

3-Inverting Power Drivers (Clamped)



INVERTING POWER DRIVER



SEQUENCE OF OPERATION

1. INPUT DOWN, TRANSISTOR ON, OUTPUT UP.
2. INPUT UP, TRANSISTOR OFF, OUTPUT DOWN.
3. 820Ω COLLECTOR RESISTOR RETURNED TO -12 VOLTS WHEN DRIVING NEGATIVE "OR" INPUTS OF DOUBLE LEVEL LOGIC BLOCKS AND WHEN DRIVING TRIGGER AC INPUTS.

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS	
					MIN	MAX
B,R, Q	Y	INPUT		UP	-0.65	-0.10
				DOWN	-7.14	-5.84
A,D, P	Y	OUTPUT		UP	-0.65	-0.10
				DOWN	-6.06	-6.8

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	10.0☆☆	50.0☆
TURN OFF	14.0☆☆	35.0☆

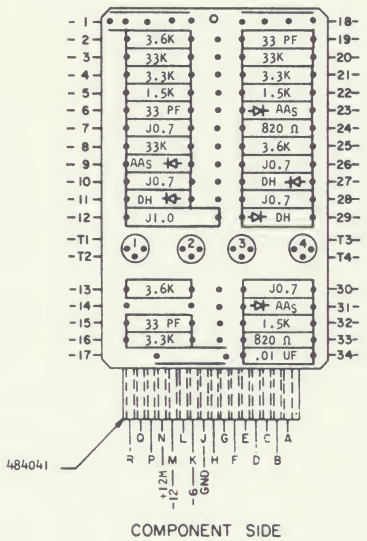
☆ASSUMES LOAD OF 10 LOGIC BLOCKS AND TR INPUT OF 70 NSEC AND INPUT TF OF 135 NSEC.

☆☆ASSUMES LOAD OF 4 LOGIC BLOCKS AND INPUT TR OF 35 NSEC AND INPUT TF OF 70 NSEC.

RISE TIME	16.0	70.0# TO 110.0##
FALL TIME	75.0	125.0## TO 190.0#

#OCCURS WHEN DRIVING TRIGGERS.

##OCCURS WHEN DRIVING LOGIC BLOCKS.

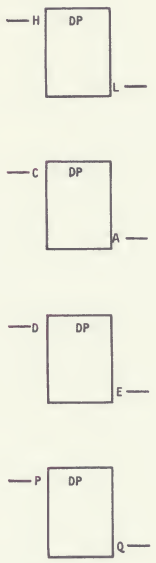


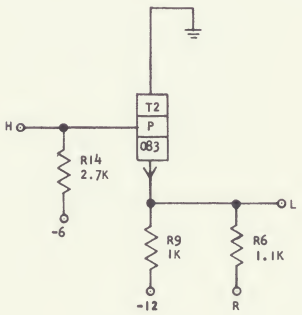
COMPONENT SIDE

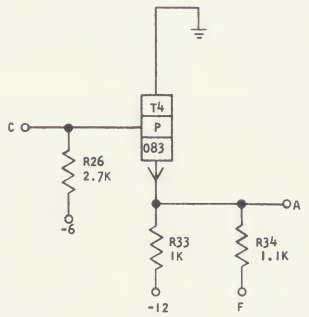
P/N 370226
DFR-

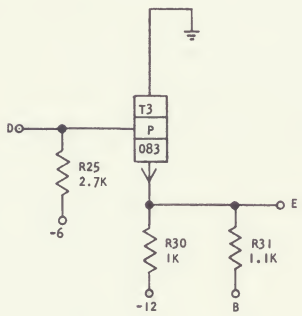
4-Emitter Followers (Non-Inverting Power Drivers)

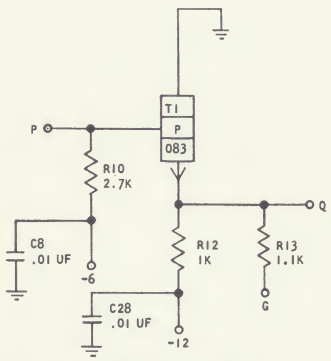
Ref. Eng. Spec. 892226











SEQUENCE OF OPERATION

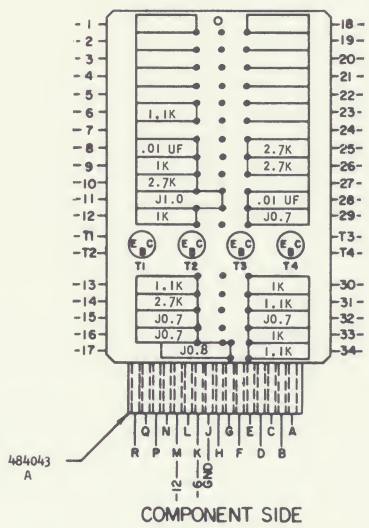
1. OUTPUT WILL FOLLOW INPUT
2. PINS R, F, B, AND G MAY BE CONNECTED TO PIN M (-12) FOR CERTAIN APPLICATIONS.

PINS		SIGNAL NAME	WAVE SHAPE		LEVELS MIN	LEVELS MAX
H,C, D,P	Y	INPUT		UP	-0.65	-0.10
				DOWN	-5.81	-8.8
L,A, E,Q	Y	OUTPUT		UP	-1.10	-0.22
				DOWN	-7.30	-5.83

DELAY - NSEC

	MINIMUM	MAXIMUM
TURN ON	6.0	20.0
TURN OFF	6.0	28.0

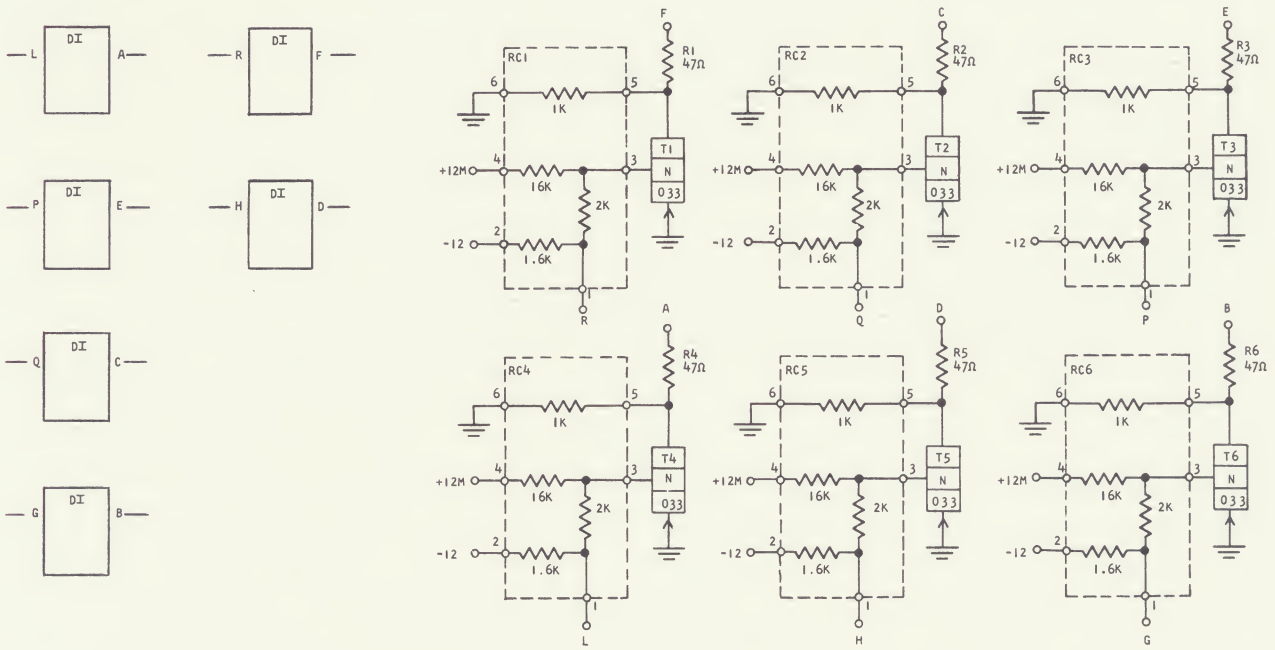
OUTPUT RISE AND FALL TIMES ARE WITHIN ±10 NSEC'S OF THE INPUT RISE AND FALL TIMES, RESPECTIVELY.



COMPONENT SIDE

P/N 370347
DGS-
Ref. Eng. Spec. 892347

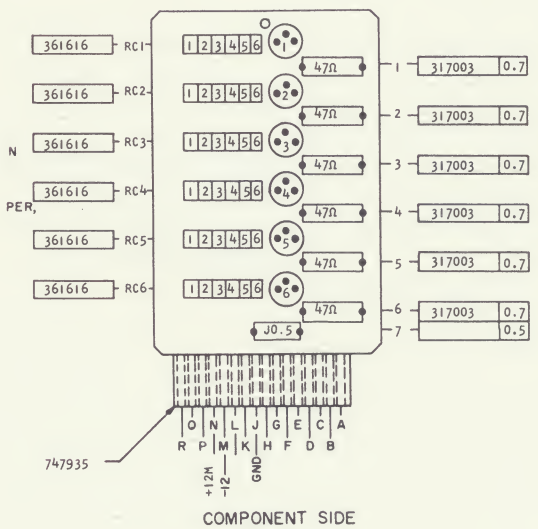
6-Indicator Drivers, 40 MA.



SEQUENCE OF OPERATION

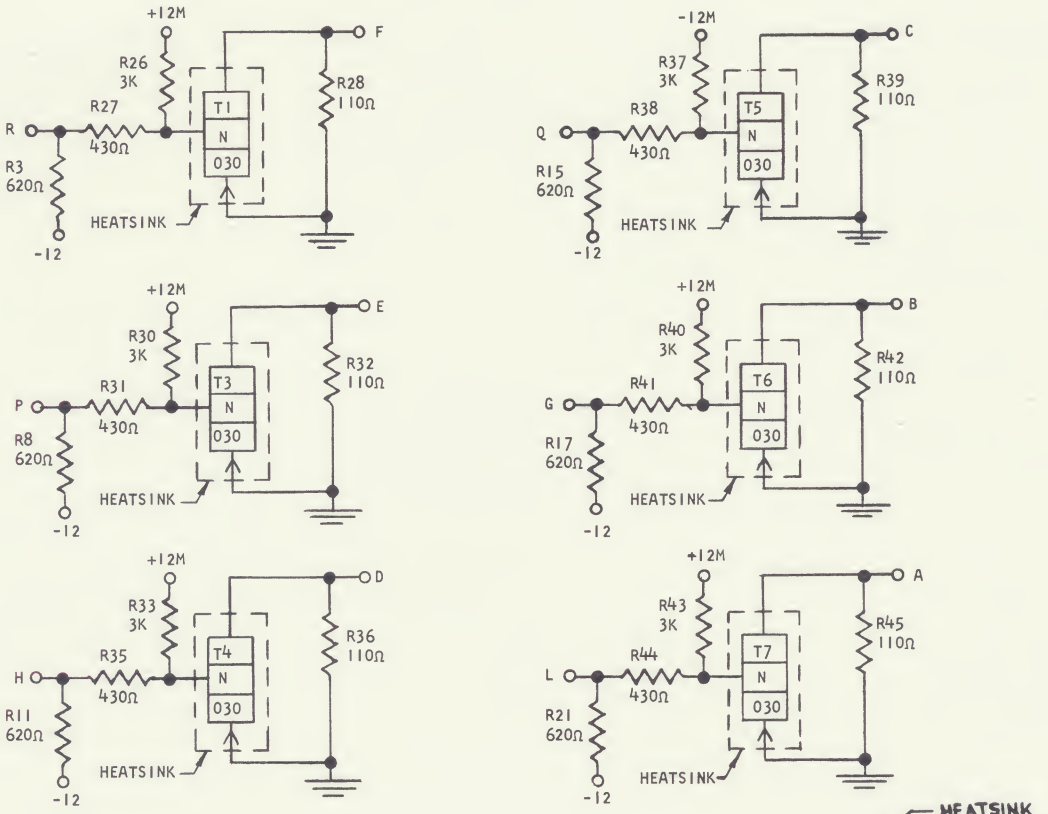
1. INPUT COWN TRANSISTOR ON OUTPUT UP
2. INPUT UP TRANSISTOR OFF OUTPUT DOWN

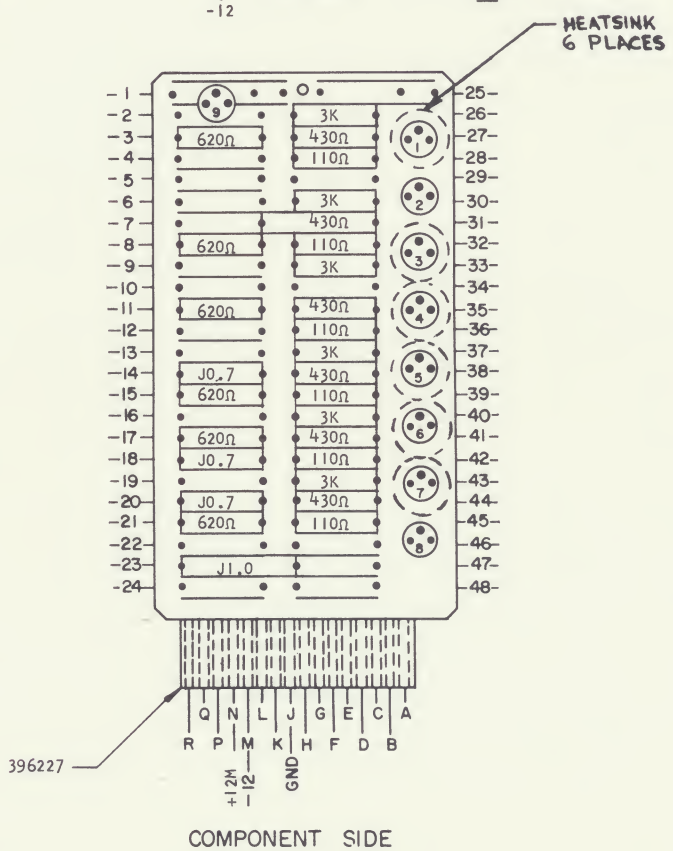
PINS	SIGNAL NAME		WAVE SHAPE		LEVELS MIN	LEVELS MAX
L,R, P,H, Q,G	Y	INPUT		UP	-0.65	0.10
				DOWN	-5.81	-7.64
A,F, E,D, C,B	S	OUTPUT		UP	-1.67	
				DOWN	-9.62	



P/N 374710
EVS-
Ref. Eng. Spec. 893550

6-Indicator Drivers, 180 MA.

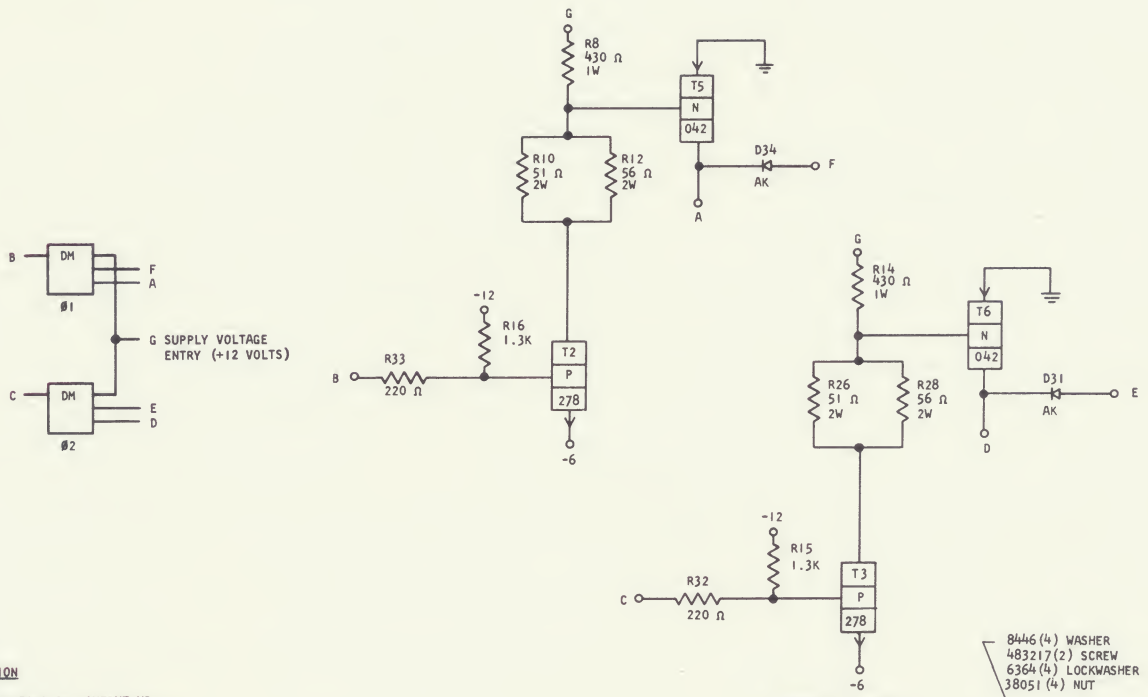




COMPONENT SIDE

P/N 372245
ASQ-
Ref. Eng. Spec. 870245

2-Relay/Solenoid Drivers



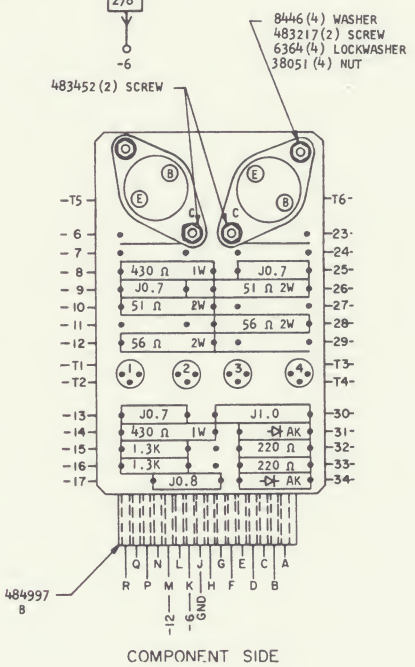
SEQUENCE OF OPERATION

1. INPUT UP: TRANSISTORS ON, OUTPUT UP.
2. INPUT DOWN: TRANSISTORS OFF, OUTPUT DOWN.

PINS	SIGNAL NAME		WAVESHAPE	LEVELS	MIN	MAX
B,C	Y	INPUT		UP	-.65V	-.05V
				DOWN	-5.81V	-12V
A,D	V	OUTPUT		UP	-.8V	+.24V
				DOWN	-18V	-22V
F,E		CLAMP		UP	-12V	-12V
				DOWN	-12V	-12V

DELAY

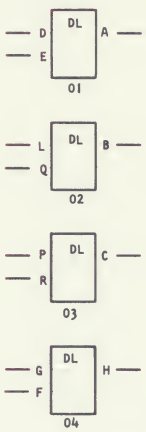
TURN ON (USEC) 1
TURN OFF (USEC) 30

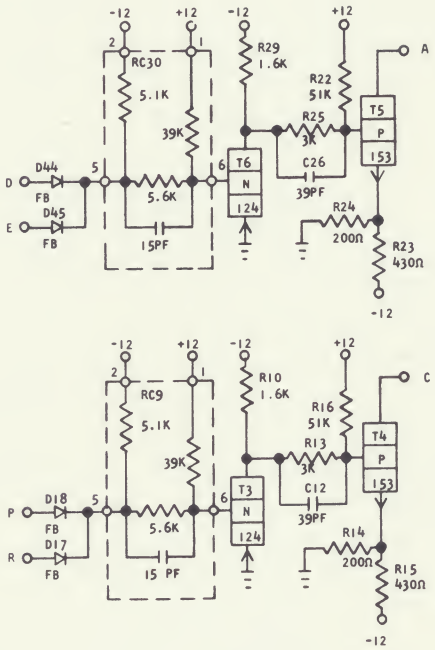


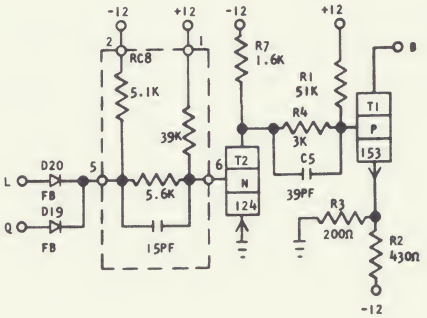
COMPONENT SIDE

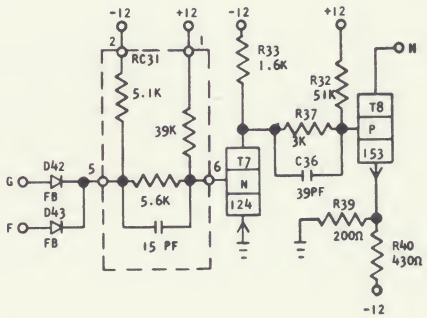
P/N 372976
UGT-
Ref. Eng. Spec. 870976

4-Line Drivers, Non-Inverting









CIRCUIT OPERATION

1. EITHER INPUT UP, OUTPUT TRANSISTOR OFF, OUTPUT UP.
2. BOTH INPUTS DOWN, OUTPUT TRANSISTOR ON, OUTPUT DOWN.

PINS	SIGNAL NAME		WAVE SHAPE	LEVELS	MIN.	MAX.
D,L P,G	Y	INPUT		UP	-0.65V	-0.05V
				DOWN	-5.81V	-12.48V
E,Q R,F	Y	INPUT		UP	-0.65V	-0.05V
				DOWN	-5.81V	-12.48V
A,B C,H		OUTPUT		UP	OUTPUT OPEN CIRCUIT LEVEL DEPENDS ON TERM.	
				DOWN	-1.25V	-1.76V

DELAY - NS

TURN ON DELAY

WITH SDTDL OR SDTRL RECEIVER

120 + C

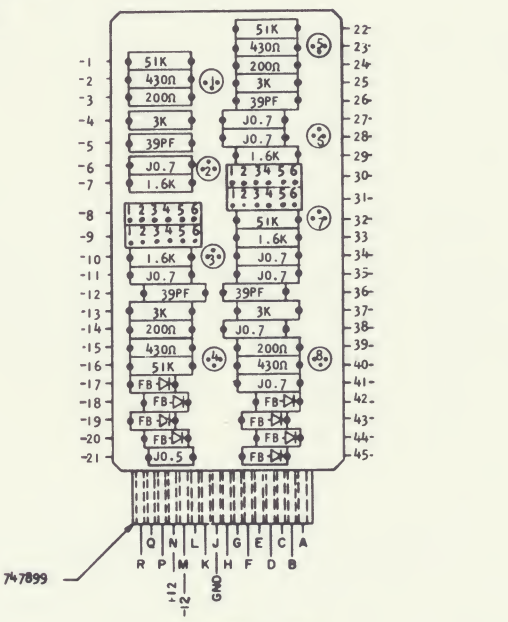
TURN OFF DELAY

SDTDL OR SDTRL RECEIVER

110 + C

WHERE C = DELAY INTRODUCED BY CABLE. ADD 2 NS PER FOOT OF CABLE.

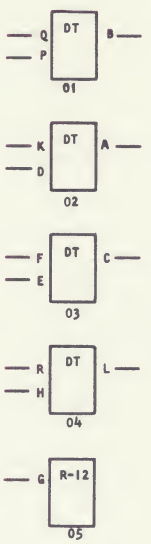
NOTE: DELAYS MEASURED FROM INPUT OF DRIVER TO OUTPUT OF TERMINATING CIRCUIT

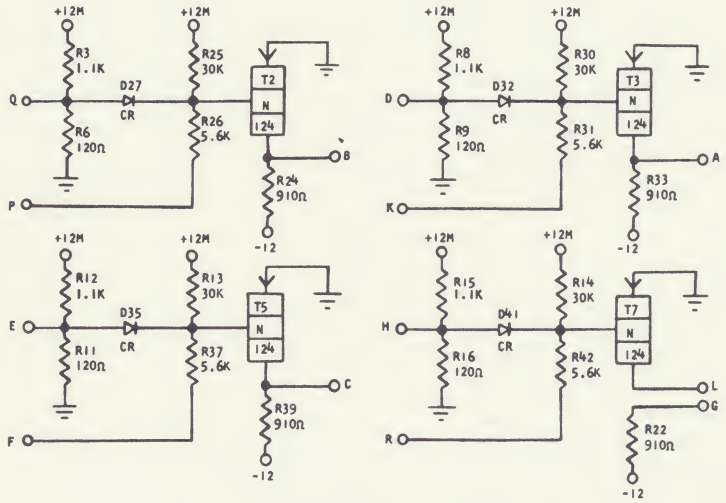


COMPONENT SIDE

4-Line Terminators, Gated

P/N 372723
YYN-
Ref. Eng. Spec. 870976





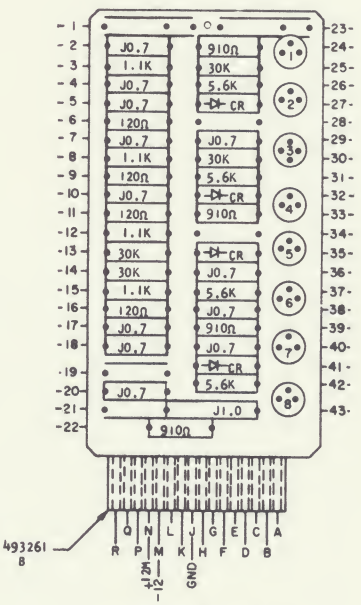
CIRCUIT OPERATION

1. LINE INPUT (PINS Q,D,E,H) HAS NO CONTROL UNLESS GATE (PINS P,K,F,R) IS AT DOWN LEVEL
2. WHEN GATE IS AT DOWN LEVEL, A DOWN LEVEL ON THE LINE INPUT CAUSES THE TRANSISTOR TO TURN ON GIVING A POSITIVE OUTPUT
3. PIN G IS A 910 Ω 1/2 WATT RESISTOR RETURNED TO -12 VOLTS AVAILABLE AS A LOAD FOR CONF. 04, OR ANY APPLICATION REQUIRING A 910 Ω RESISTOR TO -12 VOLTS.

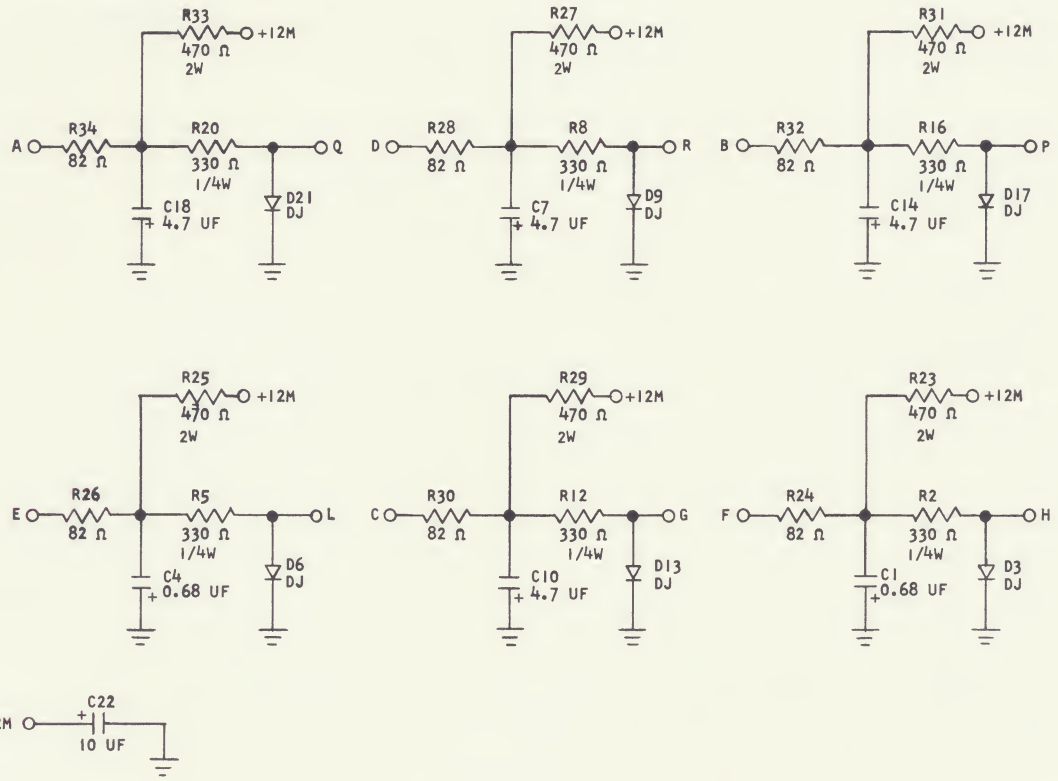
PINS		SIGNAL NAME	WAVE SHAPE	LEVEL		
					MIN	MAX
Q,D E,H	C	LINE INPUT		UP	+0.55V	+3.26V
				DOWN	-0.5V	-5.3V
P,K F,R		GATE INPUT		UP	-0.80V	+1.68V
				DOWN	-5.3V	-10.8V
B,A C,L		OUTPUT		UP	-0.05V	-0.45V
				DOWN	-5.81V	-12.48V

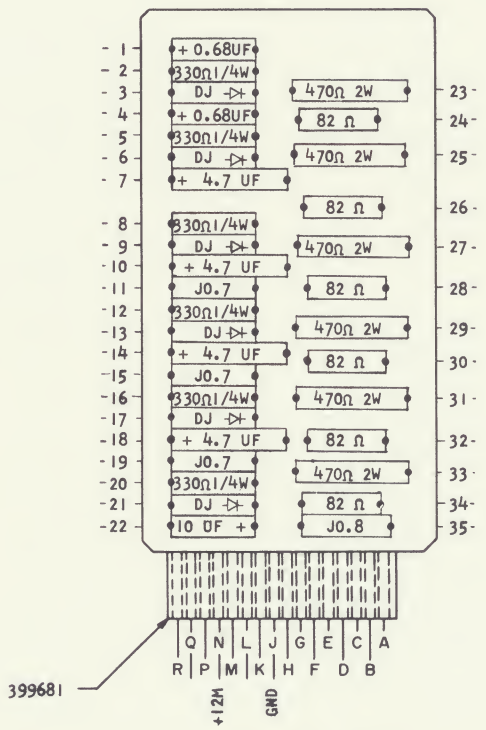
DELAY

	MAX
TURN ON (NSEC)	65
TURN OFF (NSEC)	95



COMPONENT SIDE



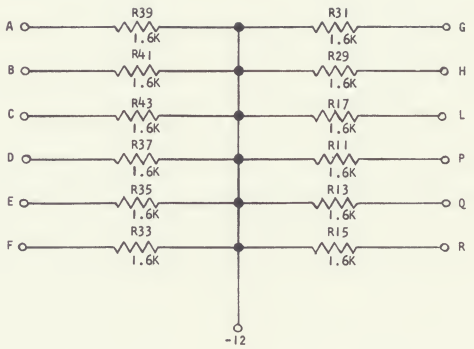


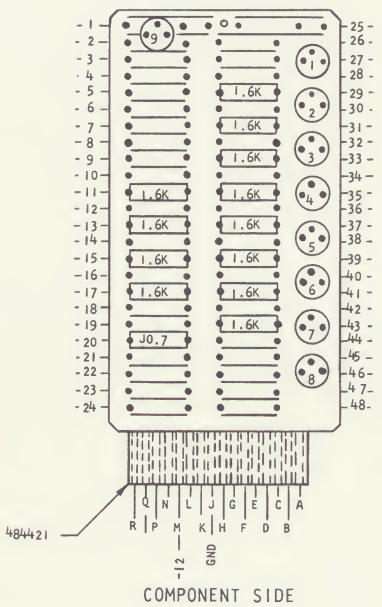
COMPONENT SIDE

P/N 370232
DFJ-

12-1.6K Load Resistors

Ref. Eng. Spec. None



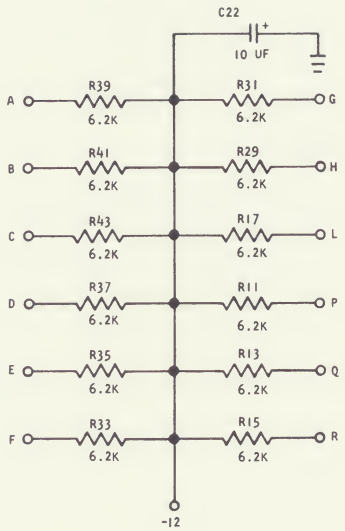


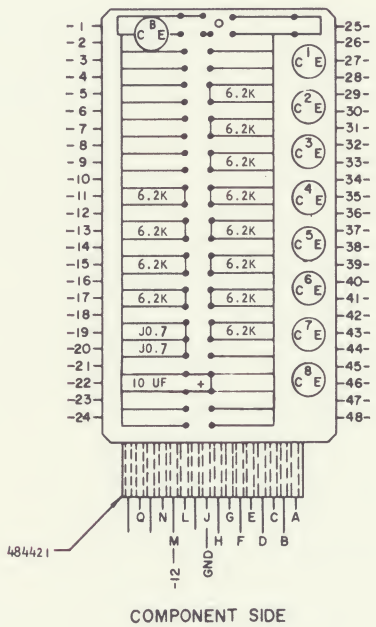
COMPONENT SIDE

P/N 370643
AJW-

12-6.2K Load Resistors

Ref. Eng. Spec. None





COMPONENT SIDE